Seat No.: _____ Enrolment No._____

GUJARAT TECHNOLOGICAL UNIVERSITY

BE - SEMESTER–III EXAMINATION – SUMMER 2016

Subject Code:130701 **Date:04/06/2016**

Subject Name:Digital Logic Design

Time:10:30 AM to 01:00 PM **Total Marks: 70**

Instructions:

1. **Attempt all questions.**
2. **Make suitable assumptions wherever necessary.**
3. **Figures to the right indicate full marks.**

Q.1	**(a)**	Explain r's complement with example in detail.	**07**
	(b)	Explain (r-1)'s complement with example in detail.	**07**
Q.2	**(a)**	Explain Excess 3 code and 2421 code in detail.	**07**
	(b)	Listout and explain the most common postulates used to formulate various algebraic structures.	**07**
		OR	
	(b)	Discuss canonical and standard forms in detail.	**07**
Q.3	**(a)**	What is positive and negative logic? Explain in detail.	**07**
	(b)	Simplify the Boolean function, F= A'C+A'B+AB'C+BC.	**07**
		OR	
Q.3	**(a)**	Simplify the Boolean function, F= A'B'C'+B'CD'+A'BCD'+AB'C'.	**07**
	(b)	Simplify the Boolean function, F=∑(0,1,2,5,8,9,10).	**07**
Q.4	**(a)**	Implement the function F=∑(0,6) with NAND gates only.	**07**
	(b)	Implement the function F=∑(0,6) with NOR gates only.	**07**
		OR	
Q.4	**(a)**	Explain Full Adder in detail.	**07**
	(b)	Prepare BCD to excess 3 code converter.	**07**
Q.5	**(a)**	Discuss PLA in detail.	**07**
	(b)	Discuss edge triggered flip flop in detail.	**07**
		OR	
Q.5	**(a)**	Explain 3 bit binary counter with necessary diagrams.	**07**
	(b)	Explain different types of random access memories.	**07**

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