Seat No.: _____ Enrolment No._____

GUJARAT TECHNOLOGICAL UNIVERSITY

BE - SEMESTER–IV EXAMINATION – SUMMER 2016

Subject Code:141101 **Date:03/06/2016**

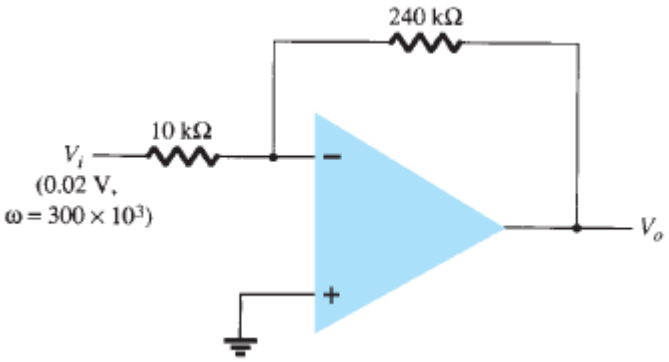
Subject Name:Advance Electronics

Time:10:30 AM to 01:00 PM **Total Marks: 70**

Instructions:

1. **Attempt all questions.**
2. **Make suitable assumptions wherever necessary.**
3. **Figures to the right indicate full marks.**

Q.1	**(a)**	Compare different types of power amplifier based on conduction angle, position of Q-point, efficiency, distortion, and application.	**07**
	(b)	For Dual slop integrator type ADC 1 Draw basic circuit 2 Explain its working 3 List its advantages over other type of ADCs. 4 List it's applications	**07**
Q.2	**(a)**	Draw the hybrid -л model for a transistor in CE configurations and explain it. Derive the equation for transconductance g_m.	**07**
	(b)	Draw the block diagram of operational amplifier and explain it in detail.	**07**
		OR	
	(b)	Draw op-amp based Wien bridge oscillator. Obtain frequency of oscillation and discuss amplitude stabilization for the same.	**07**
Q.3	**(a)**	What are the fundamental different between an amplifier and oscillator? Explain concept of oscillation with Barkhausen criteria.	**07**
	(b)	A 5-bit R-2R ladder network with logic '0'=0V and logic '1'=5V. Find i) Analog output due to LSB change ii) Full scale output voltage iii) Analog output for digital input 11100.	**07**
		OR	
Q.3	**(a)**	Explain voltage series, voltage shunt, current series and current shut feedback in brief.	**07**
	(b)	Write a short note on two stage RC-coupled amplifier.	**07**
Q.4	**(a)**	Explain cascaded amplifier and also derive the expression for the overall gain in decibels of an n-stage cascaded amplifier and why to express gain in dB?	**07**
	(b)	Describe the operation of successive approximation ADC with neat sketch.	**07**
		OR	
Q.4	**(a)**	Explain Clapp oscillator using transistor and FET.	**07**
	(b)	Determine the voltage gain, input, and output impedance with feedback for voltage series feedback having A= -100, R_i= 10 kΩ, R_0=20kΩ for feedback of i) β =0.1 and ii) β = -0.5.	**07**
Q.5	**(a)**	For the signal and circuit of figure below, determine the maximum frequency that may be used. Op-amp slew rate is SR = 0.5 V/μs.	**07**



(b) Draw and explain the working principle of crystal controlled oscillator. **07**

OR

Q.5 **(a)** Sketch the circuit of a crystal controlled oscillator. **07**

(b) Tabled the compare of TTL,CMOS, and ECL logic families based on speed, fan-in, fan-out, noise immunity, power dissipation, and application. **07**

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