Seat No.: _____ **Enrolment No._____**

GUJARAT TECHNOLOGICAL UNIVERSITY

BE - SEMESTER–VI- EXAMINATION – SUMMER 2016

Subject Code:161004 **Date:17/05/2016**

Subject Name:VLSI Technology and Design

Time: 10:30 AM to 01:00 PM **Total Marks: 70**

Instructions:

1. **Attempt all questions.**
2. **Make suitable assumptions wherever necessary.**
3. **Figures to the right indicate full marks.**

Q.1	**(a)**	Define following operating regions for the MOS system with suitable energy band diagrams: (a) Accumulation (b) Depletion (c) Inversion	**07**
	(b)	Derive the expression of threshold voltage of an n-channel MOSFET.	**07**
Q.2	**(a)**	Draw CMOS inverter circuit, its VTC and derive V_{IH} and V_{IL} .	**07**
	(b)	Explain the Simplified design flow Y-chart in VLSI.	**07**
		OR	
	(b)	Calculate the threshold voltage V_{TO} at V_{SB} = 0, for a polysilicon gate n-channel MOS transistor, with the following parameters: substrate doping density $N_A = 10^{16}$ cm^{-3}, polysilicon gate doping density $N_D = 2 \times 10^{20}$ cm^{-3}, gate oxide thickness t_{ox}= 500 A^0, and oxide-interface fixed charge density $Nox = 4 \times 10^{10}$ cm^{-2}.	**07**
Q.3	**(a)**	Derive the expression of τ_{PLH} of a CMOS inverter.	**07**
	(b)	Discuss various packaging technologies in VLSI.	**07**
		OR	
Q.3	**(a)**	Derive the expression of Switching power dissipation of CMOS inverter.	**07**
	(b)	Consider a CMOS inverter circuit with the following parameters: V_{DD} = 3.3 V, $V_{T}o,n$ = 0.6 V $V_{T}o,p$ = - 0.7 V, Kn = 200 µA/V^2 , Kp = 80 µA/V^2 . Calculate the noise margins of the circuit.	**07**
Q.4	**(a)**	Explain the voltage bootstrapping in Dynamic logic circuits.	**07**
	(b)	Draw the combinational logic circuit using nMOS for the following Boolean expression: (i) Z_1 = (A(B+C) + DE)' (ii) Z_2= ((A+D+E)+(BC))'	**07**
		OR	
Q.4	**(a)**	Write a short notes on (i)Causes of Latch up (ii) FPGA	**07**
	(b)	Discuss possible sources of noise in input and output circuits	**07**
Q.5	**(a)**	Explain the Built-In-Self-Test techniques to test VLSI circuit.	**07**
	(b)	Draw the circuit diagram of a CMOS edge-triggered D-latch and explain.	**07**
		OR	

Q.5	**(a)**	Write a short note on small device geometry effects	**07**
	(b)	Explain the functioning of CMOS transmission gate.	**07**

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