Seat No.: _____ Enrolment No._____

GUJARAT TECHNOLOGICAL UNIVERSITY

BE - SEMESTER–VII EXAMINATION – SUMMER 2016

Subject Code:172007 Date:05/05/2016

Subject Name:Modern Control Systems (Department Elective - I)

Time:02:30 PM to 05:00 PM Total Marks: 70

Instructions:

1. **Attempt all questions.**
2. **Make suitable assumptions wherever necessary.**
3. **Figures to the right indicate full marks.**

Q.1 (a) Discuss the compensation characteristic of cascade lead compensators using root locus plots.Show that Lead compensator is suitable for systems having unsatisfactory transient response, and provides a limited improvement in steady state performance. **07**

(b) A unity feedback system has forward path transfer function **07**

$$G(s) = \frac{k}{s(s+1)}$$

It is required that the closed loop poles be located at $s_{1,2}$=-1.6±j4 using a lead compensator with transfer function D(s)= $\frac{s+2.5}{s+\alpha}$.

Determine the values of α and k to locate the closed-loop poles as required.

Q.2 (a) Discuss Lag compensator is suitable for systems with satisfactory transient response but unsatisfactory steady-state response. **07**

(b) The controlled plant of a unity feedback system is **07**

$$G(s) = \frac{k}{s(s+10)^2}$$

It is specified that velocity error constant of the system be equal to 20, while the damping ratio of the dominant roots be 0.707.

Design a suitable lag compensator for the given system.

OR

(b) Controlled plant of a unity-feedback system is **07**

$$G(s)=\frac{1}{s^2+1}$$

Design a PD controller such that the dominant closed loop poles are located at -1±j√3.What is the position error constant of the compensated system?

Q.3 (a) Discuss the design step for constructing phase lead compensator using bode plot. **07**

(b) Consider the plant is given by **07**

$$G(s) = \frac{k}{s(s+2)}$$

Design a cascade lead compensator so that the closed loop system has

Phase Margin ≥ 60 and Kv ≥ 10.

OR

Q.3 (a) Discuss the design step for constructing phase lag-lead compensator using bode plot. **07**

(b) Consider a type-I unity feedback system with an open loop system transfer function **07**

$$G(s)=\frac{k}{s(s+1)}$$

It is desired to have velocity error constant Kv=10 and Phase margin of the system be at least 45.
Design a suitable lag compensator of the system.

Q.4 **(a)** Discuss the advantages of state space analysis over the classical control system. **07**

(b) Given a SISO state variable model **07**

$$\text{Prove that } \frac{Y(s)}{U(s)} = G(s) = c(sI - A)^{-1}b$$

OR

Q.4 **(a)** Explain the concept of controllability. Also derive the expression for the Controllability Test Matrix. **07**

(b) Consider a double-integrator plant described by the differential equation **07**

$$\frac{d^2\theta}{dt^2} = u(t)$$

Develop a state equation for this system with u as the input, and θ and $\dot{\theta}$ as the state variable.

Q.5 **(a)** Explain the pole placement method using state feedback control technique. **07**

(b) A regulator system has the plant **07**

$$\dot{X} = \begin{bmatrix} 0 & 1 & 0 \\ 0 & 0 & 1 \\ -6 & -11 & -6 \end{bmatrix} x + \begin{bmatrix} 0 \\ 0 \\ 1 \end{bmatrix} u$$

Design a state feedback controller which will place the closed loop poles at -2±j3.464,-5.

OR

Q.5 **(a)** Sketch a schematic diagram of a digital control system. Explain the function of each block **07**

(b) Discuss the stability analysis in a sampled data control system using Jury's stability test. **07**

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