Seat No.: _____ Enrolment No._____

GUJARAT TECHNOLOGICAL UNIVERSITY

BE - SEMESTER–VIII EXAMINATION – SUMMER 2016

Subject Code:180802 **Date:05/05/2016**

Subject Name:VLSI Technologies

Time:10:30 AM to 01:00 PM **Total Marks: 70**

Instructions:

1. **Attempt all questions.**
2. **Make suitable assumptions wherever necessary.**
3. **Figures to the right indicate full marks.**

Q.1	**(a)**	Explain VLSI design flow using Y-chart.	**07**
	(b)	Justify the statement: W/L ratio of p-MOS is 2.5 times that of n-MOS in CMOS transistor.	**07**
Q.2	**(a)**	Draw resistive load n-MOS inverter. Derive critical voltage points V_{OH}, V_{OL}, V_{IH} and V_{IL}.	**07**
	(b)	Explain basic steps of LOCOS process with neat diagram. What is bird beak region?	**07**
		OR	
	(b)	Explain n-well fabrication process for CMOS fabrication in detail with neat diagram.	**07**
Q.3	**(a)**	Calculate the threshold voltage V_{T0} at V_{SB} = 0V, for a polysilicon gate n-channel MOS transistor, with the following parameters: substrate doping density $N_A = 10^{16}$ cm^{-3}, polysilicon gate doping density $N_D = 2 \times 10^{20}$ cm^{-3}, gate oxide thickness t_{ox} = 500A° and oxide-interface fixed charge density $N_{ox} = 4 \times 10^{10}$ cm^{-2}. Assume that kT/q = 0.026 at T = 300 K.	**07**
	(b)	Define and explain the concept of regularity, modularity and locality.	**07**
		OR	
Q.3	**(a)**	What is voltage bootstrapping? Derive equation for $V_{x(max)}$ and $V_{x(min)}$.	**07**
	(b)	Write a note on CMOS ring oscillator.	**07**
Q.4	**(a)**	Explain switching power dissipation of CMOS inverter. Derive equation for average power dissipation.	**07**
	(b)	What are CMOS transmission gates? Explain its operation in detail.	**07**
		OR	
Q.4	**(a)**	Explain on-chip clock generation and its distribution in detail with neat diagram.	**07**
	(b)	Explain basic principal of pass transistor circuit. What is logic ‘1’ and logic ‘0’ transfer?	**07**
Q.5	**(a)**	Write a detailed note on ad-hoc testable technique for chip testing.	**07**
	(b)	Explain CMOS dynamic circuit techniques with example.	**07**
		OR	
Q.5	**(a)**	Write a detailed note on BIST technique for chip testing.	**07**
	(b)	Give comparison between FPGA and CPLD.	**07**

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