Seat No.: _____ Enrolment No._____

GUJARAT TECHNOLOGICAL UNIVERSITY

BE - SEMESTER–III(New) EXAMINATION – SUMMER 2016

Subject Code:2130306 Date:04/06/2016

Subject Name:Fundamentals of Digital Design

Time:10:30 AM to 01:00 PM Total Marks: 70

Instructions:

1. **Attempt all questions.**
2. **Make suitable assumptions wherever necessary.**
3. **Figures to the right indicate full marks.**

			MARKS
Q.1		**Short Questions**	**14**
	1	Convert $(ABCD)_{16}$ to decimal number.	
	2	Convert $(11010010)_2$ to octal number.	
	3	What will be odd parity of code 11001001.	
	4	What is the gary code of $(1111)_2$.	
	5	Subtract 1100 from 1111 using 1's complement method.	
	6	Draw the symbol and truth tables of AND, OR and NOT Gates.	
	7	In combinational circuit, if A and B are inputs of function F and F(A,B) = ∑(0, 1, 2, 3), what will be output? **A.** 1 **B.** 0 **C.** Both A and B **D.** None of these	
	8	In RS flip-flop if inputs s=1 and R=0, What will be output Q(t)?	
	9	Give the difference between combinational & sequential circuit.	
	10	Define Fan-out.	
	11	Draw the symbol and truth table for JK flip flop.	
	12	What is HDL & VHDL?	
	13	What is the full form of FPGA and CPLD?	
	14	In Boolean algebra, what will be output of (A+A')?	
Q.2	**(a)**	Perform (8) – (4) using 1's complement method.	**03**
	(b)	Explain binary Boolean algebra with examples.	**04**
	(c)	Explain full adder with truth table and logic diagram.	**07**
		OR	
	(c)	Explain full subtractor with truth table and logic diagram.	**07**
Q.3	**(a)**	Define universal Gates and also draw the symbol and true tables.	**03**
	(b)	Implement AND, OR and NOT gate using NAND gates.	**04**
	(c)	Design 4 bit binary parallel adder using half adder blocks.	**07**
		OR	
Q.3	**(a)**	Draw the truth table and symbol for Ex-OR and Ex-NOR gates.	**03**
	(b)	Implement AND, OR and NOT gate using NOR gates.	**04**
	(c)	Design a BCD adder using 4 bit parallel adder blocks and basic gates.	**07**
Q.4	**(a)**	Simplify the function Y(A,B,C,D) = ∑m(0,1,2,3,4,5,6,7,12,13,14,15) using K-map & draw logic diagram.	**03**
	(b)	Simplify the function Y(A,B,C,D) = ∑m(0,1,2,3,12,13,14,15) + d(8,9,10,11) using K-map & draw logic diagram.	**04**
	(c)	Design 4-bit binary to gray code converter.	**07**
		OR	
Q.4	**(a)**	Explain types of ROMs.	**03**
	(b)	Explain working of RS- flip-flop with diagram.	**04**

	(c)	Reduce the function F(w,x,y,z) = ∑m(1,5,6,12,13,14) + d(2,4) using tabulation method.	**07**
Q.5	**(a)**	Explain operation of 4:1 multiplexer with logic diagram & truth table.	**03**
	(b)	Explain Master slave flip flop with block diagram.	**04**
	(c)	Explain 4 bit Magnitude Comparator.	**07**

OR

Q.5	**(a)**	Explain state diagram with example.	**03**
	(b)	Explain successive approximation type ADC.	**04**
	(c)	Design a ripple counter and explain in detail.	**07**

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