Seat No.: _____ Enrolment No._____

GUJARAT TECHNOLOGICAL UNIVERSITY

BE - SEMESTER–III(New) EXAMINATION – SUMMER 2016

Subject Code:2131704 Date:27/05/2016

Subject Name:Digital Logic Circuits

Time:10:30 AM to 01:00 PM Total Marks: 70

Instructions:

1. **Attempt all questions.**
2. **Make suitable assumptions wherever necessary.**
3. **Figures to the right indicate full marks.**

			MARKS
Q.1		**Short Questions**	**14**
	1	(4E7)16 = ( )10	
	2	(1101110111011110 11)2 =( )16	
	3	(1011101111)2 = ( )8	
	4	(130)10 = ( )2	
	5	Give logic diagram and truth-table of EX-OR Gate.	
	6	Perform subtraction using 2's compliment of 10010 – 10011.	
	7	Convert decimal number 250 to base 7.	
	8	Convert decimal 8620 into BCD.	
	9	Define the term Accuracy.	
	10	Convert the following numbers to decimal CDA.	
	11	How many T flip flops are required to design mod-10 Asynchronous BCD counter.	
	12	Define the term fan out.	
	13	Definition of Resolution.	
	14	Define the term Monotonicity.	
Q.2	**(a)**	Draw logic diagram , graphical symbol , and Characteristic table for clocked SR flip-flop using NAND.	**03**
	(b)	Write a brief note on Master-slave flip flop with logic symbols .	**04**
	(c)	Write a brief note on Gray codes. Also discuss methods for conversion from gray to binary code and vice versa **.**	**07**
		OR	
	(c)	Explain in detail bidirectional shift register with parallel load.	**07**
Q.3	**(a)**	Convert SR flip-flop into T flip-flop**.**	**03**
	(b)	Reduce using K-mapping the expression F = Σm(1,5,6,12,13,14)+D(2,4) find out SOP and POS forms. Obtain POS minimization expression of NOR logic . Where "D" indicates Don't care conditions.	**04**
	(c)	Simplify the following Boolean function by using Tabulation method. F = Σ m(1,2,3,5,6,7,8,9,12,13,15).	**07**
		OR	
Q.3	**(a)**	Explain Associative Laws and De Morgan's theorems with necessary diagram,truth table and one example.	**03**
	(b)	Implement the boolean function F = Σ(0,1,3,4,8,9,15)with 8 × 1 multiplexer with B,C and D connected to selection lines S2,S1 and S0 respectively.	**04**
	(c)	Design sequential counter as shown in the state diagram using JK flip-flops	**07**

000 ; 001; 010; 011; 100 ; 101 ; 110 ; 111 ; 000---Clockwise direction to follow.

Q.4 **(a)** Show the hardware required to implement the following logic operations **03**

1) T1: F<—A ∧ B

2) T2:G<— C ∨ D

3) T3: E<— E ⊕F

(b) Explain 2 bit binary UP and DOWM counter using JK flip-flops. **04**

(c) Write a brief note on Successive approximation ADC. **07**

OR

Q.4 **(a)** Explain in detail binary adder and subtracter with boolean function ,k-map and truth table. **03**

(b) Explain 4-bit Magnitude Comparator in detail with necessary boolean expression. **04**

(c) Explain interfacing of a digital computer to the analog world. **07**

Q.5 **(a)** Explain in detail a 4×16 decoder constructed with two 3×8 decoders. **03**

(b) Expand A(A'+B)(A'+B+C') to min term and max term**.** **04**

(c) Explain NAND and NOR gate using RTL and DTL circuit in detail with necessary diagram and truth-table. **07**

OR

Q.5 **(a)** Show that AB'C+B+BD'+ABD'+A'C=B+C**.** **03**

(b) Write a brief note on Arithmetic micro operation in detail. **04**

(c) Explain PLA with necessary diagrams. **07**

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