Seat No.: _____ Enrolment No._____

GUJARAT TECHNOLOGICAL UNIVERSITY

BE - SEMESTER–III(New) EXAMINATION – SUMMER 2016

Subject Code:2132003 **Date:27/05/2016**

Subject Name:Design Concepts in Basic Electronics

Time:10:30 AM to 01:00 PM **Total Marks: 70**

Instructions:

1. **Attempt all questions.**
2. **Make suitable assumptions wherever necessary.**
3. **Figures to the right indicate full marks.**

MARKS

Q.1 **Short Questions** **14**

1 Which of the following gates are added to the inputs of the OR gate to convert it to the NAND gate?
A) NOT, B) AND, C) OR, D) XOR

2 The Exclusive NOR gate is equivalent to which gate following by an inverter?
A) OR, B) AND C) NAND, D) XOR

3 BCD is……
A) Binary Coded Decimal, B) Bit Coded Decimal,
C) Binary Coded Digit, D) Bit Coded Digit

4 Convert Decimal $(21)_{10}$ to Binary…….
A) $(10111)_2$, B) $(11001)_2$, C) $(11000)_2$, D) $(10101)_2$

5 Convert Binary $(11101)_2$ to decimal……..
A) $(26)_{10}$, B) $(27)_{10}$, C) $(28)_{10}$, D) $(29)_{10}$

6 A set of flip flop integrated together is called
A) Counter, B) Adder,
C) Register, D) None of the above

7 A register organized to allow to move left or right operations is called a
A) Counter, B) Coder, C) Adder, D) Shift register

8 Define Digital signal.

9 State the truth table of T-flip flop.

10 Convert $(10101)_2$ into equivalent hexadecimal.

11 Convert $(25)_8$ into equivalent decimal.

12 Define term "Register".

13 What is n-p-n transistor?

14 What is p-n-p transistor?

Q.2 **(a)** Prove the Following using truth table. **07**

(1) $$\bar{A} + \bar{B} + \bar{C} = \overline{(A \cdot B \cdot C)}$$

(2) $$XY + \bar{X}Z + YZ = XY + \bar{X}Z$$

(b) Show that NAND and NOR are universal gate. **07**

OR

	(b)	Explain Digital logic gates with symbol, algebraic function and truth table.	**07**
Q.3	**(a)**	Comparison between 1's and 2's compliments.	**03**
	(b)	Draw logic diagram and state the truth table of R-S flip-flop.	**04**
	(c)	Design 3bit up-down synchronous counters with help of T-flip flop.	**07**

OR

Q.3	**(a)**	List out digital logic families.	**03**
	(b)	Draw logic diagram and state the truth table of J-K flip-flop.	**04**
	(c)	Explain in detail different types of break down in diode.	**07**
Q.4	**(a)**	Explain forward bias circuit.	**03**
	(b)	Explain with neat diagram 8x1 multiplexer.	**04**
	(c)	Give the points of difference between half wave, full wave and bridge rectifier.	**07**

OR

Q.4	**(a)**	Explain reverse bias circuit.	**03**
	(b)	Explain with neat diagram 3 to 8 decoder.	**04**
	(c)	Explain with neat diagram working of 4-bit bidirectional shift register with parallel load.	**07**
Q.5	**(a)**	What is a clipper explain briefly.	**03**
	(b)	State the truth table of full adder and half adder.	**04**
	(c)	Explain the input output characteristics of n-p-n transistor in CB configuration. Also indicate different regions.	**07**

OR

Q.5	**(a)**	What is a clamper explain briefly.	**03**
	(b)	Draw the logic diagram and state truth table for D-flip flop.	**04**
	(c)	Explain the input output characteristics of n-p-n transistor in CE configuration. Also indicate different regions.	**07**

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