Seat No.: _____   Enrolment No._____

GUJARAT TECHNOLOGICAL UNIVERSITY
BE - SEMESTER–IV(New) EXAMINATION – SUMMER 2016

Subject Code:2140910   **Date:30/05/2016**
Subject Name:Digital Electronics
Time:10:30 AM to 01:00 PM   **Total Marks: 70**
Instructions:
1. **Attempt all questions.**
2. **Make suitable assumptions wherever necessary.**
3. **Figures to the right indicate full marks.**

Q.1		**Short Questions**	**14**
	1	$(365.24)_8 = ( )_{10}$ (a) 542.5213 b) 245.5213 c) 245.3125 d) 542.3125	
	2	In design of ripple counter using J-K flip flop the inputs of all flip flop are (a) J=1, K=1 b) J=0, K=0 c) J=0, K=1 d) J=1, K=0	
	3	$(255)_{10} = ( )_2$ (a) 11110111 (b) 11001100 (c) 11101111 (d) 11111111	
	4	If A = B = 1 then A XOR B equals _____. (a) 1 (b) 0 (c) 8 (d) 16	
	5	The compliment of previous state is known as _____. (a) Toggle (b) No-Change (c) Preset (d) Clear	
	6	Boolean identity X + X = _____. (a) 0 (b) 1 (c) X (d) X'	
	7	The output of a logic gate is '1' when all its inputs are at logic 0 (Consider 2 – inputs Gate). The gates are (a) NAND and EX-OR gate (b) NOR and EX-NOR gate (c) OR and EX-NOR gate (d) AND and EX-OR gate	
	8	The logic gate which detects equality of two bits is (a) OR (b) EX-NOR (c) NOR (d) NAND	
	9	If a 3-input NOR gate has eight input possibilities, how many of those possibilities will result in a HIGH output? (a) 1 (b) 2 (c) 7 (d) 8	
	10	Which is the fastest Analog to Digital converter (a) Flash type (b) Successive Approximation (c) Dual Slope Integrator (d) Counter type	
	11	In Binary Ladder DAC, how many resistors are used? (a) 1 (R) (b) 2 (R - 2R) (c) 3 (R-2R-3R) (d) 4 (R-2R-3R-4R)	
	12	Erasable ROM (a) ROM (b) PROM (c) EPROM (d) None of the above	
	13	Which logic family has less power consumption (a) TTL (b) ECL (c) CMOS (d) None of the above	
	14	Race around condition occurs in J-K F/F when its inputs are (a) J = 0, K = 0 (b) J = 0, K = 1 (c) J = 1, K= 0 (d) J = 1, K = 1	

Q.2	**(a)**	Perform the following subtraction by using 2's, 9's and 10's compliments. 26 – 34	**03**
	(b)	Perform the following operations. (1) 101.11 x 111.01 (2) (1110110) ÷ (101)	**04**
	(c)	Explain Hamming codes. A seven bit Hamming code is received as 1110101. What is the correct code for even parity?	**07**

OR

	(c)	Write a short note on Gray code.	**07**
Q.3	**(a)**	Define the following general characteristics of logic families.	**03**

(i) Propagation delay time (ii) Fan-in (iii) Fan - out

(b) Reduce the expression: **04**

       a) A + B (AC + (B+C') D)

       b) (A + (BC)')'(AB' + ABC)

(c) Explain two input TTL NAND gate.   **07**

OR

Q.3 **(a)** Simplify the following Boolean function using K-map   **03**

    F (w, x, y, z) = $\sum$ m(1, 3, 7, 11, 15) with don't care, d (w, x, y, z) = $\sum$m(0, 2, 5)

(b) Design NOR gate by using CMOS logic family.   **04**

(c) Simplify the following Boolean function using tabulation method   **07**

    F (w, x, y, z) = $\sum$ (0, 1, 2, 8, 10, 11, 14, 15)

Q.4 **(a)** Implement the following Boolean function by using 8:1 MUX   **03**

    F(A,B,C,D) = $\sum$m(0,1,3,4,8,9,15).

(b) Design a full adder circuit using decoder and multiplexer (4:1 MUX).   **04**

(c) Discuss 4 – bit magnitude comparator in detail.   **07**

OR

Q.4 **(a)** Discuss Left Mode serial in serial out shift register.   **03**

(b) Explain working of master-slave JK flip-flop with necessary logic diagram.   **04**

(c) Design 4 – bit synchronous up - counter (Use T flip-flop).   **07**

Q.5 **(a)** Compare various DAC techniques.   **03**

(b) Write a short note on different types of ROM.   **04**

(c) How many types of RAM? Describe the internal organization of RAM.   **07**

OR

Q.5 **(a)** State the applications of A to D converters.   **03**

(b) Explain R-2R ladder DAC network.   **04**

(c) Write down various ADC networks and explain any one in brief. Which is best ADC?   **07**

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