Seat No.: _____ Enrolment No._____

GUJARAT TECHNOLOGICAL UNIVERSITY

BE - SEMESTER–IV(New) EXAMINATION – SUMMER 2016

Subject Code:2141002 **Date:26/05/2016**

Subject Name:Analog Circuit Design

Time:10:30 AM to 01:00 PM **Total Marks: 70**

Instructions:

1. **Attempt all questions.**
2. **Make suitable assumptions wherever necessary.**
3. **Figures to the right indicate full marks.**

Q.1 Short Questions **14**

1 Why differential amplifier is necessary?
2 Why does amplifier gain reduce in BJT amplifier?
3 What is an op-amp?
4 List three open loop op-amp configurations.
5 What is the concept of Virtual ground
6 What is an instrumentation amplifier?
7 Application of voltage to current converter
8 Draw the circuit diagram of ideal op-amp
9 What is PSRR?
10 What are the applications of differentiator?
11 What do you understand by precision full wave rectifier circuit?
12 What is the major difference among SSI, MSI, LSI and VLSI ICs?
13 List the different types of voltage regulators.
14 What is error voltage?

Q.2 (a) A Hartley oscillator circuit has a tank circuit inductance of L_1=L_2=100 µH. It is required to design the oscillator to produce oscillations at50 KHz. Obtain the exact value of the tank circuit capacitance for the above said requirement. **03**

(b) Write short note on validity of hybrid-π model. **04**

(c) Explain Wien bride oscillator with neat sketch. What determines the frequency of oscillation? Will oscillations take place if the bridge is balanced? **07**

OR

(c) List the parameter those affecting to the transistor at high frequencies. Draw the hybrid π model for CE configuration and explain it. Also derived the equation for any two above listed parameter for CE configuration. **07**

Q.3 (a) What are the different important parameters of comparator circuit? **03**

(b) Define the following parameters of Op-Amp: **04**
(i) Input bias current.
(ii) Common Mode Rejection Ratio.
(iii) Input offset voltage.
(iv) Output offset voltage

(c) Derive gain equation for Op Amp for inverting and non inverting mode and derive equation for Common mode rejection Ratio (CMRR). Why CMRR should **07**

be ideally high.

OR

Q.3	**(a)**	Define slew rate of an Op-Amp .What are its causes?	**03**
	(b)	Show how Op-Amp can be used as an averaging, summing amplifiers using non inverting configuration.	**04**
	(c)	Implement an integrator using Op-Amp. Obtain the expression for the output voltage V_0.Sketch the output waveform for an input square waveform. Show the frequency response of ideal and practical integrators.	**07**
Q.4	**(a)**	Equivalent circuit of a non-inverting amplifier.	**03**
	(b)	A non inverting amplifier with a gain of 10 is to be driven with 2 volts peak to peak sine wave of 20 kHz frequency. What should be the minimum slew rate of the op-amp to have the distortion free output?	**04**
	(c)	Draw the non-inverting Schmitt trigger comparator circuit and explain the threshold levels and hysteresis.	**07**

OR

Q.4	**(a)**	What do you understand by precision rectifier?	**03**
	(b)	Comparison of linear and switching mode regulators.	**04**
	(c)	An astable multivibrator is to be designed for getting rectangular waveform with t_{ON}=0.6 ms. Draw the circuit diagram with various component values. Also calculate frequency of oscillations and duty cycle. Assume total time period (T) to be 1 ms. Assume C=0.1µs	**07**
Q.5	**(a)**	State the properties of Butterworth filter	**03**
	(b)	What is thermal drift? How does it affect the performance of an op-amp circuit?	**04**
	(c)	Design a high pass filter with a cut off frequency of 10KHz with a pass band gain of 1.5. Also plot the frequency response for the designed filter. C=0.02µF	**07**

OR

Q.5	**(a)**	Define PSRR of an op-amp .In an op-amp PSRR is 150µV/V. If supply voltage is changed from +10V to +12V, what is the change in input offset voltage Vio?	**03**
	(b)	What is the difference between active and passive filter.	**04**
	(c)	Explain wide band-pass filter with necessary circuit, derivation and waveforms	**07**