Seat No.: _____ Enrolment No._____

# GUJARAT TECHNOLOGICAL UNIVERSITY

**BE - SEMESTER–IV(New) EXAMINATION – SUMMER 2016**

**Subject Code:2142405** **Date:30/05/2016**

**Subject Name:Analog Electronics and Its Applications**

**Time:10:30 AM to 01:00 PM** **Total Marks: 70**

**Instructions:**

1. **Attempt all questions.**
2. **Make suitable assumptions wherever necessary.**
3. **Figures to the right indicate full marks.**

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| **Q.1** | | **Do as directed:-** | **14** |
| | **1** | Draw Half wave rectifier circuit. | |
| | **2** | Define PIV w.r.t. diode. | |
| | **3** | What is Op-Amp? | |
| | **4** | Define Slew rate w.r.t. Op-Amp. | |
| | **5** | Define Rectification efficiency w.r.t. diode. | |
| | **6** | Draw output waveform of Centre tap full wave rectifier. | |
| | **7** | Define PSRR w.r.t. Op-Amp. | |
| | **8** | Explain the concept of Clamper circuit. | |
| | **9** | Define Noise Margin. | |
| | **10** | What is Digital to Analog Convertor? | |
| | **11** | What are logic gates? | |
| | **12** | Draw clipper circuit. | |
| | **13** | Draw Pin diagram of OP-AMP. | |
| | **14** | Define Notch filter. | |
| **Q.2** | **(a)** | State the condition on 1+Aß which a feedback amplifier must satisfy in order to be stable. | **03** |
| | **(b)** | Draw & explain single stage transistor amplifier. | **04** |
| | **(c)** | Compare CE, CB, and CC configuration of BJT in tabular form. | **07** |
| | | **OR** | |
| | **(c)** | Draw the hybrid-pi model for a transistor in CE Configuration and discuss it. | **07** |
| **Q.3** | **(a)** | What do you understand by virtual ground concept? For a given OP-AMP CMRR = $10^5$ and differential gain $A_d = 10^5$. Determine $A_{CM}$, the common mode gain of OP-AMP. | **03** |
| | **(b)** | Write a note on: - Ideal OP-AMP characteristics. | **04** |
| | **(c)** | Explain Cascaded Amplifier and also Derive the expression for the overall gain in decibels of an n-stage cascaded amplifier and why to express gain in dB? | **07** |
| | | **OR** | |
| **Q.3** | **(a)** | Define Filter. Differentiate Active & Passive Filter. | **03** |
| | **(b)** | Explain concept of Zero Crossing Detector. | **04** |
| | **(c)** | Explain 78xx and 79xx voltage regulators. Draw necessary figures and draw circuit diagram to get 12 volt constant output using 7812 IC. | **07** |
| **Q.4** | **(a)** | Draw the circuit diagram & waveforms for saw tooth wave generator. | **03** |

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|---|---|---|---|
| | **(b)** | Draw the block diagram and connection diagram of 555 timers. | **04** |
| | **(c)** | Draw the block diagram of a linear regulated power supply and explain its working. | **07** |
| | | **OR** | |
| **Q.4** | **(a)** | Draw & explain block diagram of PLL. | **03** |
| | **(b)** | Explain working of successive approximation ADC with suitable numerical example. | **04** |
| | **(c)** | Explain summing, scaling & Averaging amplifier for inverting configuration. | **07** |
| **Q.5** | **(a)** | Write a technical note on:-Negative Impedance converter. | **03** |
| | **(b)** | What is need of Schmitt trigger circuit? Enlist & explain comparator characteristics. | **04** |
| | **(c)** | Explain Wien bride oscillator with neat sketch. What determines the frequency of oscillation? Will oscillations take place if the bridge is balanced? | **07** |
| | | **OR** | |
| **Q.5** | **(a)** | Draw the block diagram of V to F converters. | **03** |
| | **(b)** | Give the complete Classification of Oscillators. | **04** |
| | **(c)** | Compare DTL, TTL & RTL in tabular forms. | **07** |

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