Seat No.: _____ **Enrolment No._____**

GUJARAT TECHNOLOGICAL UNIVERSITY

BE - SEMESTER–V (NEW) - EXAMINATION – SUMMER 2016

Subject Code:2151007 **Date:13/05/2016**

Subject Name:Digital Design

Time:02:30 PM to 05:00 PM **Total Marks: 70**

Instructions:

1. **Attempt all questions.**
2. **Make suitable assumptions wherever necessary.**
3. **Figures to the right indicate full marks.**

Q.1	**(a)**	Explain major steps involved in digital design using CAD tools.	**07**
	(b)	Do as directed. (1)Discuss physical data type with examples as used in VHDL. (2)How to describe digital circuit using RTL. (3) State importance of configuration. (4) What is the difference between STD_LOGIC and STD_ULOGIC? (5)What do you mean by Primitive? (6)Explain any one shift operator with example. (7) Is this statement x<=y after 5 ns synthesized or not? Justify answer.	**07**
Q.2	**(a)**	Explain different abstraction level of Digital design. Also give difference between top-bottom and bottom-top methodologies for digital design.	**07**
	(b)	(1) What is difference between signal and variable with example? (2)Give difference between software language and Hardware language.	**07**
		OR	
	(b)	What do you mean by Delta-delay? Also explain Inertial Delay model and Transport Delay model.	**07**
Q.3	**(a)**	Write a HDL code (VHDL/verilog) 4 – Bit full – adder using behavioral modeling.	**07**
	(b)	Explain configuration and package declaration statements using necessary examples.	**07**
		OR	
Q.3	**(a)**	Write a HDL code (VHDL/verilog) for ALU for different operations.	**07**
	(b)	Using structural modeling implement 9bit parity generator using HDL code (VHDL/verilog).	**07**
Q.4	**(a)**	What is FPGA? Draw its basic structure and give its applications.	**07**
	(b	Draw a state diagram for moore type finite state machine which generates output ‘1’ when receives input string sequence ‘111’ on three subsequent clock cycles. Include Reset signal which bring FSM to initial state when it goes to high. Write HDL code (VHDL/verilog) code for this FSM using process statement.	**07**
		OR	
Q.4	**(a)**	Give difference between Moore FSM and Mealy FSM. Draw Moore FSM for BCD counter. Also write HDL code (VHDL/verilog) code for BCD Counter using Moore FSM model.	**07**

	(b)	Explain different wait statements. What will be the effect of including 'wait for 0 ns' statement within the middle of process statement which has signal assignments statements before and after this wait statement? Explain with appropriate example.	**07**
Q.5	**(a)**	Explain Assertion statement. Explain its usefulness in writing testbench	**07**
	(b)	Write a HDL code (VHDL/verilog) code for 3X8 decoder.	**07**
		OR	
Q.5	**(a)**	Write a HDL code (VHDL/verilog) code for Ripple counter (Modulo – 16) counter with neat Circuit Diagram, Truth table and waveforms.	**07**
	(b)	Explain Package and library with suitable example.	**07**

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