Seat No.: _____ **Enrolment No._____**

GUJARAT TECHNOLOGICAL UNIVERSITY

BE - SEMESTER–VI (NEW) - EXAMINATION – SUMMER 2016

Subject Code:2160709 **Date:17/05/2016**

Subject Name: Embedded & VLSI Design

Time: 10:30 AM to 01:00 PM **Total Marks: 70**

Instructions:

1. **Attempt all questions.**
2. **Make suitable assumptions wherever necessary.**
3. **Figures to the right indicate full marks.**

Q.1	**(a)**	Explain step by step fabrication of n-well CMOS along with necessary figures.	**07**
	(b)	Classify Embedded systems along with their applications.	**07**
Q.2	**(a)**	Derive drain current equation for n-channel MOSFET in linear mode.	**07**
	(b)	Explain different types of processors used in Embedded systems.	**07**
		OR	
	(b)	Explain parallel, serial and wireless communication interface using at least one example for each interface.	**07**
Q.3	**(a)**	Explain different operation modes of MOS with figures.	**07**
	(b)	Explain various types of Embedded system memories.	**07**
		OR	
Q.3	**(a)**	Explain semi custom Design and Full custom Design along with circuit performance and technology window.	**07**
	(b)	Write a short note on built in self test.	**07**
Q.4	**(a)**	Derive equation of V_{IL} and V_{IH} for n-type MOSFET inverter with depletion type load.	**07**
	(b)	Write a brief note on Unified Modeling Language (UML).	**07**
		OR	
Q.4	**(a)**	Define and discuss Latch-up problem in CMOS inverter. Mention causes for latch-up and guidelines for avoiding latch-up.	**07**
	(b)	Define controllability and observability. List out electrical and logical faults observed in circuit.	**07**
Q.5	**(a)**	Define sequential circuits and implement CMOS clocked JK latch.	**07**
	(b)	Give a brief note on different phases of Embedded Development Life Cycle.	**07**
		OR	
Q.5	**(a)**	Implement the function F = (A (B+C) + DE)' in CMOS.	**07**
	(b)	Consider a CMOS inverter circuit with the following parameters: V_{DD} = 3.3 V, For NMOS $V_{TO,n}$ = 0.6 V, $\mu_n C_{ox}$=60 $\mu A/V^2$, $(W/L)_n$=8 For PMOS $V_{TO,p}$ = -0.7 V, $\mu_p C_{ox}$=25 $\mu A/V^2$, $(W/L)_p$=12. Calculate noise margin of the circuit.	**07**

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