Seat No.: _____ **Enrolment No._____**

GUJARAT TECHNOLOGICAL UNIVERSITY

BE - SEMESTER–VI (NEW) - EXAMINATION – SUMMER 2016

Subject Code:2161004 **Date:17/05/2016**

Subject Name: VLSI Design

Time: 10:30 AM to 01:00 PM **Total Marks: 70**

Instructions:

1. **Attempt all questions.**
2. **Make suitable assumptions wherever necessary.**
3. **Figures to the right indicate full marks.**

Q.1	**(a)**	Explain Fabrication of n-MOSFET	**07**
	(b)	Explain different packaging technology	**07**
Q.2	**(a)**	Draw i/p and o/p waveform during high to low transition of o/p for CMOS inverter and derive expression for $\tau_{PHL.}$ using differential equation method.	**07**
	(b)	Explain procedure to measure tranconductance (K), Vto and Modulation coefficient (λ) MOSFET parameters.	**07**
		OR	
	(b)	Derive drain current using gradual channel approximate	**07**
Q.3	**(a)**	Draw the Inverter circuit with Resistive Load. Derive critical voltage points V_{OH}, V_{OL}, V_{IL} and V_{IH} for Resistive Load Inverter circuit. Shows the effect of KnR_L value on transfer characteristics.	**07**
	(b)	Design a resistive load inverter with R_L=1KΩ, such that V_{OL} = 0.6V. The enhancement type driver transistor has the following parameters: V_{dd} = 5V, V_{To} = 1V, γ = 0.2 $V^{1/2}$, λ =0, $\mu_n C_{ox}$ = 22 $\mu A/V^2$. Determine i) Require aspect ratio. W/L ii) V_{IL} and V_{IH} and iii) noise margin NM_L and NM_H	**07**
		OR	
Q.3	**(a)**	Draw CMOS Inverter circuit and voltage transfer characteristics. Mention different operating region of NMOS and PMOS on VTC and derive critical voltage V_{IL} and V_{IH} equation.	**07**
	(b)	Consider a CMOS inverter with the following parameters: V_{Ton} = 0.6 V, V_{Top} = - 0.7 V ,K_n' = 50 uA/V^2, K_p' = 16 uA/V^2, $(W/L)_n$ = 4, $(W/L)_p$ = 5 Calculate the noise margins of this circuit. The power supply voltage is V_{DD} = 3.3 V.	**07**
Q.4	**(a)**	Explain elmore delay analysis using example to find delay of interconnect node.	**07**
	(b)	Justify importance of transmission gate. Realize following functions using TG. i) F=AB+A'C'+AB'C and ii) Six transistor implementation of 2 input XOR gate using TG.	**07**
		OR	
Q.4	**(a)**	Implement the following Boolean function using CMOS F=[(C+D+E)(B+A)]' find a equivalent CMOS inverter circuit simultaneous switching of all inputs. Assume (W/L)p=15 for all pmos transistor and (W/L)n= 10 for all nmos transistor.	**07**
	(b)	Write a short note on Built In Self Test (BIST).	**07**
Q.5	**(a)**	Explain the behavior of bistable element with two inverter circuit and derive output voltage equation.	**07**
	(b)	Discuss Ad Hoc testability design techniques in detail.	**07**

OR

Q.5	**(a)**	Draw CMOS implementation of D latch with two inverter and two CMOS TG gates. Explain its working.	**07**
	(b)	Write short note on MOSFET capacitances.	**07**

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