Seat No.: _____   Enrolment No._____

GUJARAT TECHNOLOGICAL UNIVERSITY
BE - SEMESTER–VI (NEW) - EXAMINATION – SUMMER 2016

Subject Code:2161101   **Date:13/05/2016**
Subject Name: VLSI Technology & Design
Time: 10:30 AM to 01:00 PM   **Total Marks: 70**
Instructions:
1. **Attempt all questions.**
2. **Make suitable assumptions wherever necessary.**
3. **Figures to the right indicate full marks.**

Q.1	**(a)**	Explain VLSI Design Flow.	**07**
	(b)	Derive drain current using gradual channel approximation.	**07**
Q.2	**(a)**	Derive switching power dissipation equation of CMOS inverter with idea step input.	**07**
	(b)	Derive threshold voltage equation and explain what is substrate bias effect.	**07**

OR

(b) Calculate the threshold voltage Vto at Vsb=0, for a polysilicon gate n-channel MOS transistor, with the following parameters: substrate doping density $Na=10^{16}$ cm^{-3}, plysilicon gate doping density $N_D = 10^{20}$ cm^{-3}, gate oxide thickness $t_{ox} = 500$ A^o and oxide interface fixed charge density $N_{ox} = 2X10^{10}$ cm^{-2}, Thermal voltage $=KT/q=0.026V$, energy gap of silicon (Eg) = 1.12eV, $ni = 1.45x10^{10}$ cm^{-3}, $\varepsilon_o = 8.85x10^{-14}$ F/cm, $\varepsilon_{ox} = 3.97 \varepsilon_o$ and $\varepsilon_{si} = 11.7\varepsilon_o$ **07**

Q.3 **(a)** Draw CMOS Inverter circuit and voltage transfer characteristics. Mention different operating region of NMOS and PMOS on VTC and derive critical voltages V_{IL} and V_{IH} equation.   **07**

(b) Consider a CMOS inverter with the following parameters: **07**
$V_{Ton} = 0.6$ V, $V_{Top} = - 0.7$ V, $K_n' = 50$ uA/V^2, $K_p' = 16$ uA/V^2, $(W/L)_n = 4$, $(W/L)_p = 5$ Calculate the noise margins of this circuit. The power supply voltage is $V_{DD} = 3.3$ V.

OR

Q.3 **(a)** Draw the Inverter circuit with Resistive Load. Derive critical voltage points V_{OH}, V_{OL}, V_{IL} and V_{IH} for Resistive Load Inverter circuit. Shows the effect of KnR_L value on transfer characteristics.   **07**

(b) Design a resistive load inverter with $R_L=1K\Omega$, such that $V_{OL} = 0.6V$. The enhancement type driver transistor has the following parameters: **07**
$V_{dd} = 5V$, $V_{To} = 1V$, $\gamma = 0.2$ V$^{1/2}$, $\lambda =0$, $\mu_nC_{ox} = 22$ μA/V^2.
Determine i) Require aspect ratio. W/L ii) V_{IL} and V_{IH} and iii) noise margin NM_L and NM_H

Q.4 **(a)** Implement the following Boolean function using CMOS F=[(C+D+E)(B+A)]' find a equivalent CMOS inverter circuit simultaneous switching of all inputs. Assume (W/L)p=15 for all pmos transistor and (W/L)n= 10 for all nmos transistor.   **07**

(b) Justify importance of transmission gate. Realize following functions using TG.   **07**
    i) F=AB+A'C'+AB'C and

    ii) F=AB' + A'B

OR

Q.4 **(a)** Draw i/p and o/p waveform during high to low transition of o/p for CMOS inverter and derive expression for $\tau_{PHL.}$ using differential equation method.   **07**

(b) Write a short note on Built In Self Test(BIST).   **07**

Q.5 **(a)** What is the need of voltage bootstrapping? Discuss voltage bootstrapping in detail. **07**

(b) Draw the circuit diagram of domino CMOS logic gate and discuss it in detail. **07**

OR

Q.5 **(a)** Draw CMOS implementation of D latch with two inverter and two CMOS TG gates. Explain its working. **07**

(b) Draw the gate and circuit level CMOS SR latch based on NOR2 gate and discuss it in detail. **07**

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