Seat No.: _____ Enrolment No._____

GUJARAT TECHNOLOGICAL UNIVERSITY

BE – SEMESTER – VI EXAMINATION – WINTER 2015

Subject Code:161004 **Date:14/12/ 2015**

Subject Name: VLSI Technology and Design

Time:2:30pm to 5:00pm **Total Marks: 70**

Instructions:

1. **Attempt all questions.**
2. **Make suitable assumptions wherever necessary.**
3. **Figures to the right indicate full marks.**

Q.1 **(a)** Derive the expression of threshold voltage of an n-channel MOSFET. **07**

(b) Consider the n-channel enhancement-type MOSFET shown below.The process parameters are given as follows: **07**

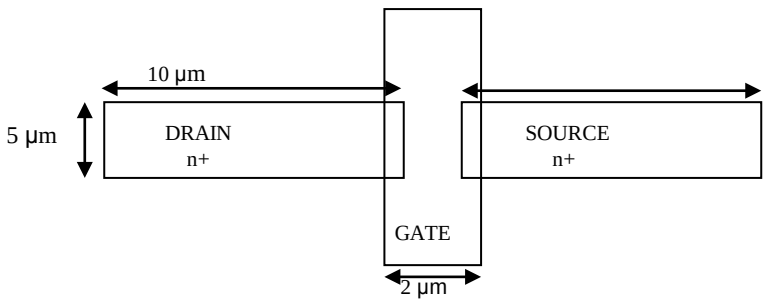
Substrate doping $N_A = 2 \times 10^{15}$ cm^{-3}

Source/drain doping $N_D = 10^{19}$ cm^{-3}

Sidewall (p+) doping N_A (sw) = 4×10^{16} cm^{-3}

Gate oxide thickness tox = 45 nm

Junction depth xj = 1.0 μm



The substrate is biased at 0V.Assume that the drain voltage is changing from 0.5 V to 5 V , find the average drain-substrate junction capacitance Cdb.

Q.2 **(a)** Discuss the effect of Full scaling(constant-Field scaling) on: **07**
(i) C_{ox} (ii) I_D (iii) P (iv) Power Density

(b) Explain the following: **07**
(i)Channel length modulation
(ii)Substrate bias effect

OR

(b) Draw a typical test circuit arrangement for the measurement of kn , V_{TO} and γ of an n-channel MOSFET. Explain how the parameters are measured. **07**

Q.3 **(a)** Define the critical voltage levels of an inverter and also define the noise margins of an inverter. **07**

(b) Derive the expression of τ_{PHL} of a CMOS inverter. **07**

OR

Q.3 **(a)** Derive the expression of V_{OH},V_{OL},V_{IL},V_{IH} of a resistive-load inverter. **07**

(b) Prove that oscillation frequency of a CMOS ring oscillator is inversely proportional to the propagation delay of the inverter. **07**

Q.4 **(a)** Write a short note on CMOS Transmission gate. **07**

	(b)	Draw the circuit diagram of a CMOS edge-triggered D-latch and explain.	**07**

OR

Q.4	**(a)**	Explain the estimation of interconnect parasitics.	**07**
	(b)	Discuss the effect of charge storage and charge leakage in pass transistor circuits.	**07**
Q.5	**(a)**	Discuss the on-chip clock generation and distribution.	**07**
	(b)	Explain the basic process flow of fabrication of the n-MOS transistor with neat sketches.	**07**

OR

Q.5	**(a)**	Discuss various packaging technology used for VLSI chips.	**07**
	(b)	Explain the Built-In-Self-Test techniques to test VLSI circuit.	**07**

****