Seat No.: _____ Enrolment No._____

GUJARAT TECHNOLOGICAL UNIVERSITY

BE - SEMESTER–VII EXAMINATION – WINTER 2015

Subject Code: 172403 **Date:09/12/2015**

Subject Name: Power Processing Circuits - II

Time: 10:30am to 1:00pm **Total Marks: 70**

Instructions:

1. **Attempt all questions.**
2. **Make suitable assumptions wherever necessary.**
3. **Figures to the right indicate full marks.**

Q.1	**(a)**	Explain applications of multilevel inverter as active & reactive power compensation.	**07**
	(b)	Describe working of active front end rectifier. Discuss effect of source inductance on input current waveform.	**07**
Q.2	**(a)**	Draw & explain basic series inverter circuit employing load commutation. State limitation of this series inverter.	**07**
	(b)	Explain principle of phase angle control for 1-phase AC voltage controller. Derive equation for RMS value of output voltage waveform.	**07**
		OR	
	(b)	Describe the function of 3-phase to 1-phase cycloconverter circuit with necessary diagrams.	**07**
Q.3	**(a)**	Draw block diagram of online UPS system. Explain each block in detail.	**07**
	(b)	Explain circuit of auxiliary commutated 1-phase bridge inverter with relevant waveforms.	**07**
		OR	
Q.3	**(a)**	Enlist various types of batteries used in UPS system. Also give comparison between constant current, constant voltage & trickle charging system.	**07**
	(b)	Explain modified McMurry – Bedford half bridge inverter circuit with related voltage & current waveforms.	**07**
Q.4	**(a)**	With an appropriate power diagram, discuss the principle of working of a 3 phase inverter with 180° conduction mode. Draw waveforms for line voltages & phase voltages.	**07**
	(b)	Enlist various control strategy for inverter. Discuss input side & output side control strategy for 1-phase inverter.	**07**
		OR	
Q.4	**(a)**	Define parallel resonance. Explain the concept of parallel resonant inverter circuit with required diagrams.	**07**
	(b)	What is PWM? Explain unipolar SPWM technique. Also compare it with bipolar SPWM technique.	**07**
Q.5	**(a)**	Explain 3 level diode clamped multilevel inverter (DCMLI) with necessary diagrams. Also write merits & demerits of it.	**07**
	(b)	Write a short note on SVPWM.	**07**
		OR	
Q.5	**(a)**	Draw circuit diagram of 7 level asymmetric cascaded H-bridge multilevel inverter. Explain how 7 levels is generated across the pole terminal.	**07**
	(b)	Define the term harmonic. State demerits of it & discuss selective harmonic elimination scheme in brief.	**07**

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