Seat No.: _____ Enrolment No._____

GUJARAT TECHNOLOGICAL UNIVERSITY

BE - SEMESTER–VIII EXAMINATION – WINTER 2015

Subject Code:180802 Date:04/12/2015

Subject Name: VLSI Technologies

Time: 2:30pm to 5:00pm Total Marks: 70

Instructions:

1. **Attempt all questions.**
2. **Make suitable assumptions wherever necessary.**
3. **Figures to the right indicate full marks.**

Q.1	**(a)**	Explain the VLSI design flow by Y-chart and its simplified view.	**07**
	(b)	Discuss basic steps of the LOCOS Process.	**07**
Q.2	**(a)**	Explain the fabrication steps of nMOS transistor with necessary figures	**07**
	(b)	Explain the MOS system under external bias.	**07**
		OR	
	(b)	Explain energy band diagram of MOS structure at surface inversion and derive the equation of threshold voltage.	**07**
Q.3	**(a)**	Derive the expression for drain current as a function of V_{GS}, V_{DS} and V_{SB} for all three region of operation of MOSFET using Gradual Channel Approximation.	**07**
	(b)	Explain two different down scaling techniques for MOSFET. Which technique is preferable?	**07**
		OR	
Q.3	**(a)**	Write a short note on MOSFET Capacitance.	**07**
	(b)	Give the delay time definitions and calculation of delay times.	**07**
Q.4	**(a)**	Explain the functioning of depletion load nMOS inverter and derive critical voltage points V_{OH}, V_{OL}, V_{IL} and V_{IH}.	**07**
	(b)	Draw the CMOS inverter circuit and VTC for different operating regions of the nMOS and PMOS transistor. Derive V_{OH}, V_{OL}, V_{IH} and V_{IL}.	**07**
		OR	
Q.4	**(a)**	Explain the design of symmetric CMOS and show that $(W/L)_p = 2.5 (W/L)_n$ for unity KR value.	**07**
	(b)	Discuss n-well process in detail.	**07**
Q.5	**(a)**	Explain the Concept of Regularity, Modularity and Locality.	**07**
	(b)	Compare full custom design and standard cell based design techniques	**07**
		OR	
Q.5	**(a)**	Write a short note on Built In Self Test (BIST).	**07**
	(b)	Explain the basic principle of pass transistor circuit. Explain logic “1” transfer and logic “0” transfer.	**07**

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