Seat No.: _____ Enrolment No._____

GUJARAT TECHNOLOGICAL UNIVERSITY

BE - SEMESTER–III (New) EXAMINATION – WINTER 2015

Subject Code:2130306 **Date:29/12/2015**

Subject Name: Fundamentals of Digital Design

Time: 2:30pm to 5:00pm **Total Marks: 70**

Instructions:

1. **Attempt all questions.**
2. **Make suitable assumptions wherever necessary.**
3. **Figures to the right indicate full marks.**

			MARKS
Q.1		**Short Questions**	**14**
	1	What do you mean by digital signal?	
	2	$(241.75)_{10} = (\_\_\_\_\_)_2$	
	3	$(47.25)_8 = (\_\_\_\_\_)_{10}$	
	4	$(1101101.1100111)_2 = (\_\_\_\_\_)_{16}$	
	5	Define Fan-out.	
	6	Give the difference between combinational & sequential circuit.	
	7	Give the classification of logic devices.	
	8	Explain Noise margin in digital circuit.	
	9	Draw symbol & truth table for RS-flip-flop.	
	10	What do you mean by resolution in terms of D/A converter?	
	11	Prove universality of NAND gate.	
	12	Define propagation delay in digital circuit.	
	13	What is HDL & VHDL?	
	14	Define FPGA & CPLD.	
Q.2	**(a)**	Perform (-9) – (-5) using 2's complement method.	**03**
	(b)	State & explain De Morgan's theorems.	**04**
	(c)	Implement the function $F = W(X + YZ) + X\bar{Y}$ using NOR gates.	**07**
		OR	
	(c)	Implement the function $F = (A + \bar{B})(CD + E)$ using NAND gates.	**07**
Q.3	**(a)**	Design full subtractor circuit using half subtractor.	**03**
	(b)	Simplify the function Y = ∑m(1,2,7,12,13) + d(0,5,15) using K-map & draw logic diagram.	**04**
	(c)	Design 4-bit binary to gray code converter.	**07**
		OR	
Q.3	**(a)**	Explain full adder with truth table & logic diagram.	**03**
	(b)	Reduce the function F(w,x,y,z) = ∑m(1,5,6,12,13,14) + d(2,4) using tabulation method.	**04**
	(c)	Design a combinational circuit whose input is 3-bit binary number & output binary number is square of input.	**07**
Q.4	**(a)**	Explain types of ROMs.	**03**
	(b)	With logic diagram & truth table explain 3 to 8 line decoder.	**04**
	(c)	A combinational circuit is defined by the function $F_1(A, B, C) = \sum m(3, 5, 6, 7)$ & $F_2(A, B, C) = \sum m(0, 2, 4, 7)$. Implement this circuit with a PLA having 3 inputs, 4 product terms and 2 outputs.	**07**

OR

Q.4	**(a)**	Define PLA with block diagram.	**03**
	(b)	Explain operation of 8:1 multiplexer with logic diagram & truth table.	**04**
	(c)	Explain PAL in detail with necessary diagram & compare it with PROM.	**07**
Q.5	**(a)**	Explain working of JK- flip-flop with diagram.	**03**
	(b)	Explain R-2R ladder type DAC.	**04**
	(c)	Explain Moore & Mealy model for sequential circuit.	**07**

OR

Q.5	**(a)**	What is race-around condition in JK flip-flop? How can we avoid it?	**03**
	(b)	Explain successive approximation type ADC.	**04**
	(c)	For clocked JK- flip-flop write the state table, draw the state diagram and write the state equation.	**07**

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