Seat No.: _____ Enrolment No._____

GUJARAT TECHNOLOGICAL UNIVERSITY

BE - SEMESTER–III (New) EXAMINATION – WINTER 2015

Subject Code:2131004 Date:18/12/2015

Subject Name: Digital Electronics

Time: 2:30pm to 5:00pm Total Marks: 70

Instructions:

1. **Attempt all questions.**
2. **Make suitable assumptions wherever necessary.**
3. **Figures to the right indicate full marks.**

Q.1		**Short Questions**	**14**
	1	Convert decimal number $(43)_{10}$ to binary.	
	2	Convert octal number $(234)_8$ to hexadecimal.	
	3	Which gates are also known as controlled NOT gate?	
	4	Bubbled OR is also called _____.	
	5	How many selection lines are required in 32X1 MUX?	
	6	How many enable lines are there in 3X8 decoder IC 74138?	
	7	Define fan-out.	
	8	Which flip-flop is also known as *ones-catching* flip-flop?	
	9	Which circuit is used to eliminate *chattering*?	
	10	Which latch is also known as *transparent* latch?	
	11	Calculate the number of state flip-flops required to generate 49 states?	
	12	Mention two different methods used to delay the state changes sufficiently.	
	13	What do you mean by conditional output?	
	14	What are the advantages of asynchronous state machines?	
Q.2	**(a)**	Convert decimal number $(0.252)_{10}$ to binary with an error less than 1 %.	**03**
	(b)	Minimize the following Boolean expressions. 1. X = ((A'B'C')' + (A'B)')' 2. Y = AB + ABC' + A'BC + A'BC'	**04**
	(c)	Implement following logic function using 8X1 MUX. F = ∑ m(0, 1, 3, 5, 7, 11, 13, 14, 15)	**07**
		OR	
	(c)	Design a full adder using 3X8 decoder followed by gates.	**07**
Q.3	**(a)**	Draw & explain in brief pin diagram of 7485 four-bit magnitude comparator.	**03**
	(b)	Using D as the MEV, reduce Y = A'B'C'D' + A'B'CD' + AB'C'D' + AB'C'D + AB'CD + AB'CD'.	**04**
	(c)	Minimize following Boolean function using K-map & design the simplified function using logic gates. F = ∑ m(1, 2, 4, 6, 7, 11, 15) + ∑ d(0, 3)	**07**
		OR	
Q.3	**(a)**	Draw a frequency divider using JK FFs to divide input clock frequency by a factor of 8.	**03**
	(b)	Reduce following Boolean function and then realize the reduced one using NOR gate only. X = A (B'+C') (A+D)	**04**

(c) For the figures 1, 2, & 3, plot the output waveforms referenced to the clock signal assuming the initial contents of all FFs is Q = 0. Assume all FFs are edge triggered. **07**

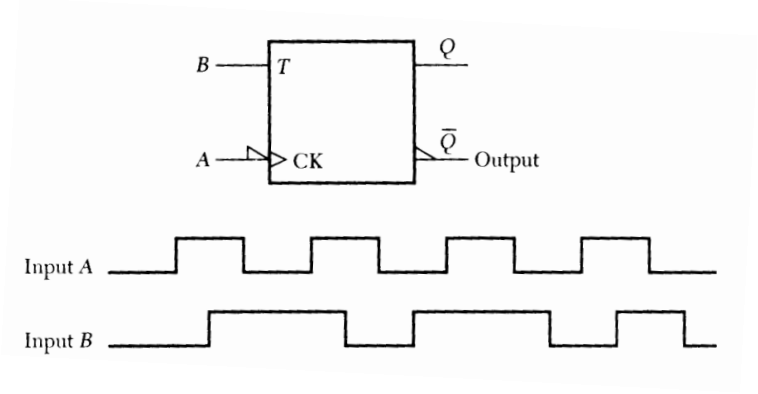

Fig. 1

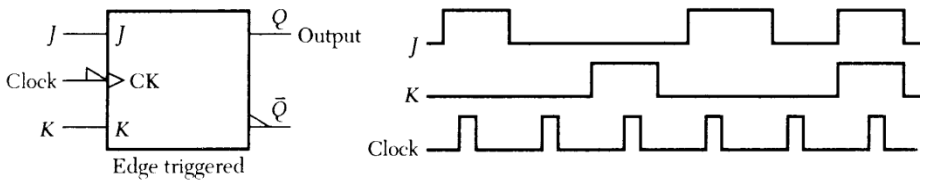

Fig. 2

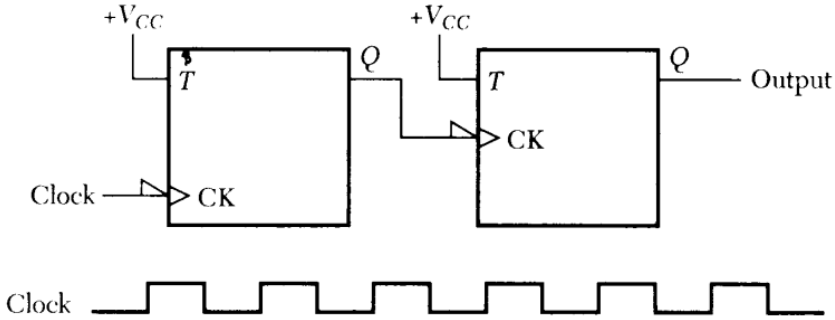

Fig. 3

Q.4 **(a)** Draw a general model for a sequential or state machine. Also list out various types of FSMs. **03**

(b) 1. Fill in values for S & R to cause the Q values of the SR FF given in figure 4. **04**

	t_0	t_1	t_2	t_3
S	0			
R	0			
Q	1	0	0	1

Fig. 4

2. Plot the output waveform for the inputs shown in figure 5, assuming the initial contents of the FF is Q = 0.

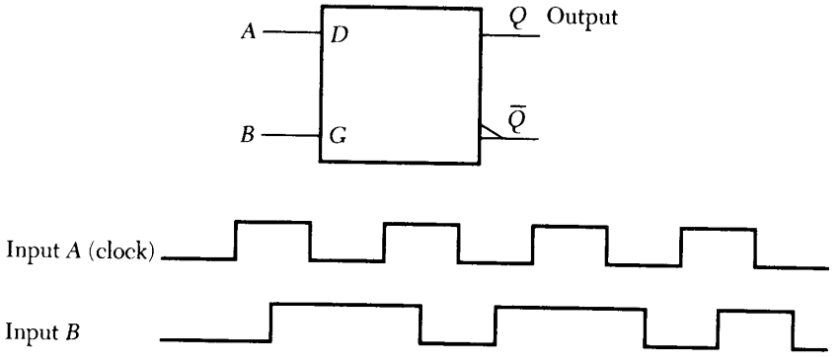

Fig. 5

(c) Design a 3-bit synchronous up counter using K-maps and positive edge-triggered JK FFs. **07**

OR

Q.4 **(a)** Draw & explain in brief a high assertion input SR latch. **03**

(b) Construct next state table for the state diagram given in figure 6. **04**

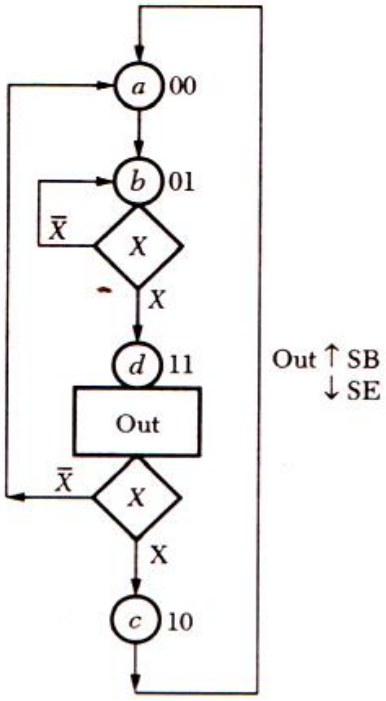

Fig. 6

(c) What do you mean by an output glitch problem? Explain any one method to eliminate the glitch from an OFL circuit. Draw suitable waveforms and logic diagrams. **07**

Q.5 **(a)** Draw & explain in brief general architecture of Xilinx FPGA. **03**

(b) Explain *critical race* problem of an asynchronous state machines with the help of one example. **04**

(c) Implement following functions using ROM. **07**

F1 = $\sum$ m(1, 3, 4, 6)
F2 = $\sum$ m(2, 4, 5, 7)
F3 = $\sum$ m(0, 1, 5, 7)
F4 = $\sum$ m(1, 2, 3, 4)

OR

Q.5 **(a)** With the help of next state D input maps given in figure 7, construct IFL using MUXs of suitable size and number. **03**

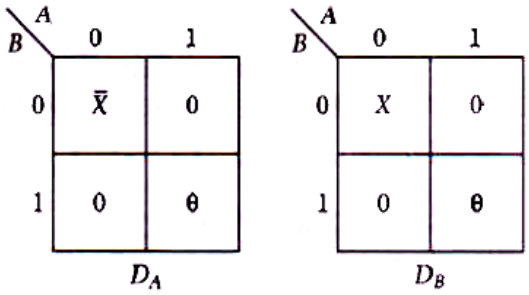

Fig. 7

(b) Explain *oscillation* problem of an asynchronous state machines with the help of one example. **04**

(c) Compare TTL, ECL, & CMOS logic families. **07**

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