Seat No.: _____ Enrolment No._____

# GUJARAT TECHNOLOGICAL UNIVERSITY

**BE - SEMESTER–IV (New) EXAMINATION – WINTER 2015**

**Subject Code:2140707 Date:30/12/2015**

**Subject Name: Computer Organization**

**Time: 2:30pm to 5:00pm Total Marks: 70**

**Instructions:**

1. **Attempt all questions.**
2. **Make suitable assumptions wherever necessary.**
3. **Figures to the right indicate full marks.**

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|---|---|---|---|
| **Q.1** | **(a)** | What do you mean by register transfer? Explain in detail. Also discuss three-state bus buffer. | **07** |
| | **(b)** | Write a detailed note on instruction cycle with neat diagrams. | **07** |
| **Q.2** | **(a)** | Explain register stack and memory stack with neat sketches. | **07** |
| | **(b)** | A computer uses a memory unit with 256K words of 32 bits each. A binary instruction code is stored in one word of memory. The instruction has four parts: an indirect bit, an operation code, a register code part to specify one of 64 registers, and an address part.<br>1. How many bits are there in operation code, the register code part, and the address part?<br>2. Draw the instruction word format and indicate the number of bits in each part.<br>3. How many bits are there in the data and address inputs of the memory? | **07** |
| | | **OR** | |
| | **(b)** | Elaborate Flynn's classification for computers. | **07** |
| **Q.3** | **(a)** | Draw a flowchart for first pass of an assembler and explain the same in brief. | **07** |
| | **(b)** | Write a note on microprogram sequencer. | **07** |
| | | **OR** | |
| **Q.3** | **(a)** | What is meant by addressing modes? List and explain any five addressing modes by taking proper example(s). | **07** |
| | **(b)** | Discuss four-segment instruction pipeline with diagram(s). | **07** |
| **Q.4** | **(a)** | Explain Booth multiplication algorithm for multiplying binary integers in signed 2's complement representation. | **07** |
| | **(b)** | Write a detailed note on Direct Memory Access (DMA). | **07** |
| | | **OR** | |
| **Q.4** | **(a)** | Write a brief note on:<br>- Subroutine call and return<br>- RISC | **07** |
| | **(b)** | Describe microprogrammed control organization in detail. | **07** |
| **Q.5** | **(a)** | Discuss associative mapping and direct mapping in organization of cache memory. | **07** |
| | **(b)** | Explain addition and subtraction operations with signed 2's complement integer data. Support your answer by taking appropriate example(s). | **07** |

**OR**

| | | | |
|---|---|---|---|
| **Q.5** | **(a)** | What do you mean by address space and memory space in virtual memory? Also explain the relation between address space and memory space in virtual memory. | **07** |
| | **(b)** | Describe cache coherence problem and its solutions in detail. | **07** |

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