| Seat No.: | Enrolment No. |
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GUJARAT TECHNOLOGICAL UNIVERSITY

Subject Code: 2151007

BE – SEMESTER – V (NEW) EXAMINATION – WINTER 2015

Date:10/12/2015

| Tiı | • | Attempt all questions. Make suitable assumptions wherever necessary. | 70 |
|-----|------------|--|----------|
| Q.1 | (a) | Write a brief note on VHDL language and the difference between programming languages and HDL. | 07 |
| | (b) | Write brief note on VHDL data types. | 07 |
| Q.2 | (a) (b) | Write a brief note on generics and configuration. Write VHDL code for 4*1 multiplexer using structural modeling. OR | 07 07 |
| | (b) | Write a VERILOG code for 3*8 decoder using gate level modeling | 07 |
| Q.3 | (a) | Explain briefly variable assignment and signal assignment statement with example. | 07 |
| | (b) | Explain process statement briefly and write VHDL code for SR FLIPFLOP using behavioral. | 07 |
| | | OR | |
| Q.3 | (a) | Explain wait statement briefly and also explain term "wait for 0ns" with waveform. | 07 |
| | (b) | Write a VHDL code for 4-bit ripple carry full adder using for loop. | 07 |
| Q.4 | (a) (b) | Write a VHDL code for pulse counter. Write a VHDL code for barrel shifter. | 07 07 |
| 0.4 | () | OR | 05 |
| Q.4 | (a) (b) | Write a VHDL code for generic priority encoder. Explain modeling of MOOREY FSM with state diagram and code. | 07 07 |
| Q.5 | (a) | Explain modeling of MEALY FSM with state diagram and code. | 07 |
| | (b) | Draw and explain digital design flow for FPGA. OR | 07 |
| Q.5 | (a) | Write a VERILOG code for NOR gate and CMOS inverter using switch level modeling. | 07 |
| | (b) | Write a short note on FPGA and also list out the difference between CPLD and FPGA. | 07 |
