

Seat No.: _____

Enrolment No.: _____

GUJARAT TECHNOLOGICAL UNIVERSITY
DIPLOMA ENGINEERING – SEMESTER – III • EXAMINATION – SUMMER 16

Subject Code: 3331703

Date: 17.05.2016

Subject Name: Digital Techniques

Time: 02:30 PM TO 05:00 PM

Total Marks: 70

Instructions:

1. Attempt all questions.
2. Make Suitable assumptions wherever necessary.
3. Figures to the right indicate full marks.
4. Use of programmable & Communication aids are strictly prohibited.
5. Use of only simple calculator is permitted in Mathematics.
6. English version is authentic.

Q.1

Answer any seven out of ten.

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1. How is a *J-K* flip-flop made to toggle?
 - A. $J = 0, K = 0$
 - B. $J = 1, K = 0$
 - C. $J = 0, K = 1$
 - D. $J = 1, K = 1$
2. Each "1" entry in a K-map square represents:
 - A. a HIGH for each input truth table condition that produces a HIGH output.
 - B. a HIGH output on the truth table for all LOW input combinations.
 - C. a LOW output for all possible HIGH input conditions.
 - D. a DON'T CARE condition for all possible input truth table combinations.
3. A decoder can be used as a demultiplexer by _____.
 - A. tying all enable pins LOW
 - B. tying all data-select lines LOW
 - C. tying all data-select lines HIGH
 - D. using the input lines for data selection and an enable line for data input
4. Convert binary 11111110010 to hexadecimal.
 - A. EE_{16}
 - B. FF_{16}
 - C. $2FE_{16}$
 - D. FD_{16}
5. Determine odd parity for each of the following data words:
1011101 11110111
 - A. $P = 1, P = 1$
 - B. $P = 0, P = 0$
 - C. $P = 1, P = 1$
 - D. $P = 0, P = 0$
6. Asynchronous counters are often called _____ counters.
 - A. toggle
 - B. ripple
 - C. binary
 - D. flip-flop
7. A logic circuit that provides a HIGH output for both inputs HIGH or both inputs LOW is a(n):
 - A. Ex-NOR gate
 - B. OR gate
 - C. Ex-OR gate
 - D. NAND gate

- (b) List applications of A/D Converter in instrumentation. **04**
- (c) What is a multiplexer? Implement 4:1 line multiplexer with truth-table. **07**
- Q.5** (a) Draw any logic components for pressure loop for pressure switch configuration HL. **04**
- (b) Implement Full Adder circuit. **04**
- (c) Implement Even-Parity Generator circuit. **03**
- (d) Simplify $AB'C + ABC + AC + A'B'C$ and draw its logic diagram with minimum gates. **03**
