Seat No.: _____ Enrolment No._____

GUJARAT TECHNOLOGICAL UNIVERSITY

MCA - SEMESTER– I EXAMINATION – Summer - 2016

Subject Code: 2610004 Date: 11-05-2016

Subject Name: Fundamentals of Computer Organization

Time: 02.30pm to 05.00 pm Total Marks: 70

Instructions:

1. **Attempt all questions.**
2. **Make suitable assumptions wherever necessary.**
3. **Figures to the right indicate full marks.**

Q.1	**(a)**	Do as directed :	
		i. List main three parts of computer system.	**01**
		ii. 1010100.01001 – 110000.01010 = _____.	**01**
		iii. $(512.5)_{10}$ = (_____)$_2$.	**01**
		iv. Perform : 412.7 – 409.2 using 9's complement method.	**01**
		v. Perform : 0.1001 – 0.01101 using 1's complement method.	**01**
		vi. Convert : $(632.97)_{10}$ to its equivalent octal number.	**01**
		vii. Convert : $(101101111010)_2$ to its equivalent hex number.	**01**
	(b)	Do as directed :	
		i. Simplify : AB′C′ + A′B′C′ + A′BC′ + A′B′C	**02**
		ii. Simplify using K-map : ABC + A′B′C′ + ABC′ + AB′C	**02**
		iii. De Morganize : (A(B+C)(C′+D′))′	**02**
		iv. Give a dual of X .(X′+Y) = X . Y	**01**
Q.2	**(a)**	Write a note on scanners.	**07**
	(b)	Explain Indirect and Relative Addressing mode with suitable example.	**07**
		OR	
	(b)	Explain Direct and Indexed Addressing mode with suitable example.	**07**
Q.3	**(a)**	What is Flip-flop? Explain SR flip-flop and its functionality.	**07**
	(b)	Explain 4×1 Multiplexer.	**07**
		OR	
Q.3	**(a)**	Explain working of 3-bit counter.	**07**
	(b)	Explain design of Half – Adder Circuit.	**07**
Q.4	**(a)**	Write a note of ROM.	**07**
	(b)	Explain Instruction word with suitable examples.	**07**
		OR	
Q.4	**(a)**	Write a note on Secondary Memories.	**07**
	(b)	Explain Instruction and Execution Cycle.	**07**
Q.5	**(a)**	Write the Boolean expression (in SOP form) for a logic network with 3 inputs that will have a 1 output when X=1 irrespective of values of Y & Z. The circuit will have a 0 output for all other sets of input values. Simplify the expression derived and draw a block diagram for the simplified expression.	**07**
	(b)	Draw the block diagram of 8086 and explain queue and segment registers.	**07**
		OR	
Q.5	**(a)**	Design two level NAND-to-NAND gate network for the expression : AB′C′ + A′B′C′ + A′BC′ + A′B′C	**07**
	(b)	Explain different addressing modes of 8086 with example.	**07**

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