Seat No.: _____ Enrolment No._____

GUJARAT TECHNOLOGICAL UNIVERSITY

ME – SEMESTER II (OLD) – • EXAMINATION – SUMMER 2016

Subject Code: 1710412 **Date: 18/05/2016**

Subject Name: Digital VLSI Design

Time:10:30 am to 01:00 pm **Total Marks: 70**

Instructions:

1. **Attempt all questions.**
2. **Make suitable assumptions wherever necessary.**
3. **Figures to the right indicate full marks.**

Q.1	**(a)**	Answer the following questions in short. (Two marks each)	**14**
	1	Why CMOS is preferred compared to BJT in Digital VLSI design?	
	2	Compare static and dynamic circuit for size, power dissipation and speed of operation.	
	3	For 90nm process what is feature size and λ?	
	4	Why photo resist material is used in CMOS fabrication process?	
	5	Discuss crosstalk and its implications.	
	6	Draw circuit of Tri state buffer using CMOS gate.	
	7	In 180nm process with ratio W/L = 4/2λ NMOS transistor has a gate oxide thickness of 50A°. Calculate gate capacitance per micron of width.	
Q.2	**(a)**	Draw Circuit diagram and stick diagram for boolean function $Y = \overline{AB + C}$	**07**
	(b)	Draw energy band diagram of the combined MOS system. Explain MOS system under different external bias voltage with energy band diagram.	**07**
		OR	
	(b)	Derive and explain the Threshold voltage equation for NMOS transistor.	**07**
Q.3	**(a)**	Sketch following boolean functions using CMOS compound gate with transistor widths chosen to achieve equal effective rise and fall resistance i.e. $(W/L)_{n,\,eq}$ 1. $Y_1 = \overline{A\,(B + C) + DE}$ 2. $Y_2 = \overline{ABC}$	**07**
	(b)	Explain MOSFET Scaling.	**07**
		OR	
Q.3	**(a)**	Sketch 2 input NOR gate with transistor widths chosen to achieve effective rise and fall resistance equal to a unit inverter. Compute the rising and falling propagation delays in terms of R and C of the NOR gate driving h identical NOR gates using Elmore delay model. If C = 2fF/µm and R = 2.5KΩ • µm in a 180nm process, what is the delay of fanout-of-4 NOR gate?	**07**
	(b)	Discuss I-V characteristic of CMOS inverter with appropriate diagram and necessary equations.	**07**
Q.4	**(a)**	State importance of Power-Delay Product and explain with necessary equations.	**07**
	(b)	For depletion load inverter circuit, discuss noise margin with transfer characteristic.	**07**
		OR	
Q.4	**(a)**	For 2 input NOR gate, derive switching threshold expression.	**07**
	(b)	Explain dynamic power dissipation in CMOS inverter with diagram and waveform.	**07**
Q.5	**(a)**	With diagram explain 1 bit full adder using transmission gates.	**07**

	(b)	Discuss cascading problem in dynamic CMOS logic circuit with appropriate diagram.	**07**

OR

Q.5	**(a)**	Explain Complementary pass transistor logic (CPL). With diagram explain 2 input NOR and 2 input NAND gate using CPL.	**07**
	(b)	Write short note on NORA CMOS logic.	**07**

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