Seat No.: _____ Enrolment No._____

GUJARAT TECHNOLOGICAL UNIVERSITY

ME – SEMESTER II (OLD) – • EXAMINATION – SUMMER 2016

Subject Code: 1720302 **Date:18/05/2016**

Subject Name: Advance Instrumentation

Time:10:30 am to 01:00 pm **Total Marks: 70**

Instructions:

1. **Attempt all questions.**
2. **Make suitable assumptions wherever necessary and mention it clearly in your solution.**
3. **Figures to the right indicate full marks.**
4. **Draw all necessary circuit diagrams in your solution.**
5. **All symbols carry their usual meanings.**
6. **Show all node voltages, currents used in solution of your circuit diagram**

Q.1 Draw the circuit diagram of strain-gauge bridge, having four strain-gauges, connected with instrumentation amplifier (IA), referred to as a load cell, and having calibration facility to account for gauge resistances and reference voltage. **14**

i. Derive the relationship of output voltage with gain of IA, reference voltage, and fractional change in resistance δ.

ii. Let the strain-gauges be of 120 $\Omega \pm 1$ % types and their maximum power dissipation limited to 10 mW to avoid excessive self heating. Assume that $V_{REF} = 15V \pm 5\%$, specify suitable values for resistances R_1 through R_4 used for calibration.

iii. Outline the calibration procedure.

Q.2 **(a)** What do you mean by input bias and input offset current? Derive the equation of error voltage generated due to the input bias current and input offset current for the resistive feedback op amp circuit. What are the ways to reduce this error voltage? What are the consequences of these ways? **07**

(b) Find the gain of the circuit in figure 1 considering virtual short condition. **07**

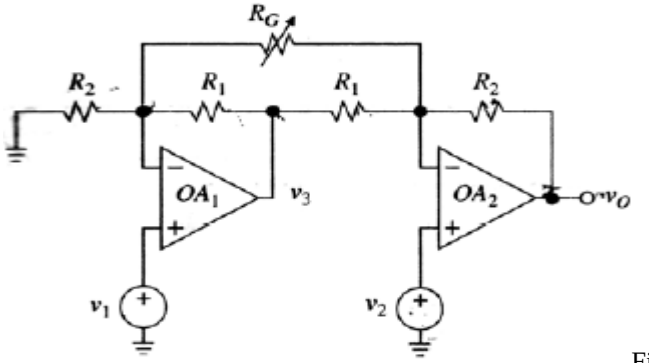

Figure 1

OR

(b) With the help of circuit diagrams, equations and Bode plot describe any two first-order active filters. **07**

Q.3 Derive the equation of feedback factor β for the circuit in figure 2 if r_d = 2 MΩ. **14**

and r0 = 75Ω. Justify whether it is positive feedback circuit or negative feedback circuit. Consider R_1=30 kΩ, R_2=20 kΩ , R_3=10 kΩ while deriving equation of feedback factor β.

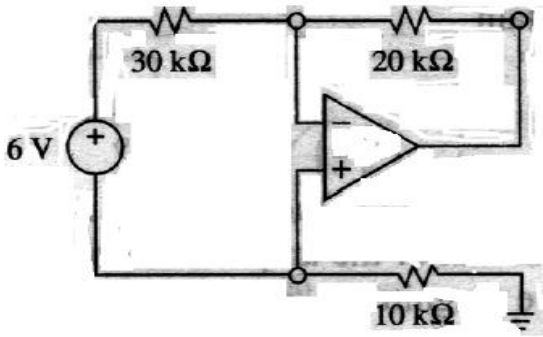

Figure 2

OR

Q.3 Draw the circuit diagrams of floating load V to I converters with (i) non-inverting and (ii) inverting configurations. Consider in both the circuits V_I=5V, R=10 kΩ , +/-Vsat = +/- 13V and a resistive load R_L. For both circuits find (i) i_0; (ii) the voltage compliance; (iii) the maximum permissible value of R_L. **14**

Q.4 Draw the circuit diagram of low pass KRC filter and derive the equations for gain, ω_0 and Q-factor. **14**

Using equal component design specify elements for a second order low pass filter with f_0=2kHz and Q=5. What is the dc gain of this design?

Modify this circuit for a dc gain of 0 dB.

OR

Q.4 **(a)** Explain slew rate with the help of necessary waveforms and derivations. An op-amp shown in figure 3 has an input bias current of 15 μA and a compensation capacitance Cc of 20 pF, and slew rate of 0.5V/μs, find its response $v_o(t)$ to a step input of -0.5 V. Consider R_1 = 2 kΩ and R_2 = 8 kΩ. **07**

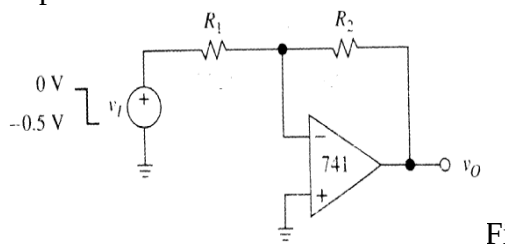

Figure 3

(b) List important features of switched capacitor filters. Discuss its practical limitations in detail. **07**

Q.5 **(a)** Explain noise power density, spectral noise density, and white noise in detail. **07**

(b) The difference amplifier shown in figure 4 uses 741 op amp and a perfectly matched resistance set with R1=10kΩ and R2=1000kΩ. Suppose the inputs are tied together and driven with a common signal v_I. Estimate the typical change in v_o if (i) v_I is slowly changed from 0 to 10V, and (ii) v_I is a 10kHz, 10V peak to peak sine wave. Consider $CMRR_{dB}$ (10kHz) = 57dB. **07**

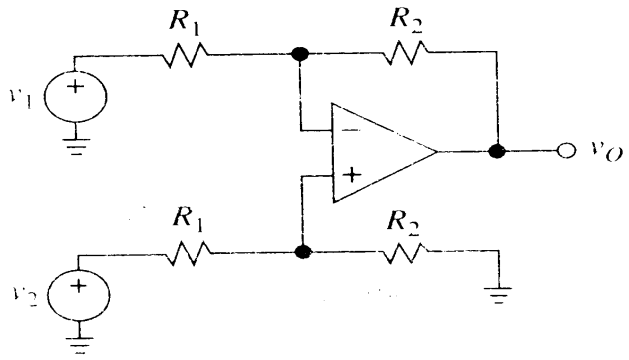

Figure 4

OR

Q.5 **(a)** A 741 op amp with ±15V supplies is configured as a non inverting amplifier having a gain of 5 V/V. (a) If the ac input amplitude is Vim=0.5V, what is the maximum frequency before the output distorts? (b) If f=10kHz, what is the maximum value of Vim before the output distorts? (c) If Vim=40 mV, what is the useful frequency range of operation? (d) If f = 2kHz, what is the useful input amplitude range? **07**

(b) With the help of circuit diagram, necessary equations and bode plot explain the effect of finite gain bandwidth product on integrator circuits. **07**

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