Seat No.: _____ Enrolment No._____

GUJARAT TECHNOLOGICAL UNIVERSITY

ME – SEMESTER I (NEW) – • EXAMINATION – SUMMER 2016

Subject Code: 2710507 **Date:17/05/2016**

Subject Name: ASIC DESIGN

Time:02:30 pm to 05:00 pm **Total Marks: 70**

Instructions:

1. **Attempt all questions.**
2. **Make suitable assumptions wherever necessary.**
3. **Figures to the right indicate full marks.**

Q.1	**(a)**	What is VHDL? List major capabilities of VHDL.	**07**
	(b)	Explain data types used in VHDL.	**07**
Q.2	**(a)**	Define Mealy State Machine and Moore State Machine. Compare them.	**07**
	(b)	What do you mean by Delta-delay? Also explain Inertial Delay model and Transport Delay model.	**07**
		OR	
	(b)	Write a short note on operators used in VHDL	**07**
Q.3	**(a)**	Draw and Explain FPGA Architecture	**07**
	(b)	Write a VHDL code for 2 x 4 Decoder using Behavioral and Dataflow style of modeling.	**07**
		OR	
Q.3	**(a)**	Write a VHDL Code for Positive Edge Triggered J K Flip Flop.	**07**
	(b)	Explain configuration and package declaration statements using necessary examples.	**07**
Q.4	**(a)**	Write a VHDL code for 4 bit Binary Up-Down counter (Modulo – 16).	**07**
	(b)	Write a VHDL code for 4x1 MUX using Behavioral and Dataflow modeling Style.	**07**
		OR	
Q.4	**(a)**	Explain the ASIC Design flow.	**07**
	(b)	Explain following terms with reference to VHDL (1) Generate Statement (2) Wait Statement (3) Generic	**07**
Q.5	**(a)**	Explain With –Select and When-Else Statements using Syntax	**07**
	(b)	Write VHDL code for 0111 sequence detector using FSM.	**07**
		OR	
Q.5	**(a)**	Write a VHDL code for 8 bit serial-in, serial-out shift register.	**07**
	(b)	Explain ROM, PAL, PLA, and PLD.	**07**

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