Seat No.: _____ Enrolment No._____

GUJARAT TECHNOLOGICAL UNIVERSITY

ME – SEMESTER I (NEW) – • EXAMINATION – SUMMER 2016

Subject Code: 2712602 **Date:17/05/2016**

Subject Name: CMOS CIRCUIT DESIGN-I

Time:02:30 pm to 05:00 pm **Total Marks: 70**

Instructions:

1. **Attempt all questions.**
2. **Make suitable assumptions wherever necessary.**
3. **Figures to the right indicate full marks.**

Q.1 **(a)** Explain in detail power consumption in CMOS Gates. Discuss Static & Dynamic power dissipation in CMOS Circuits. **07**

(b) Derive voltage gain Av, output resistance Rout and 3-db Bandwidth equations for Source follower. **07**

Q.2 **(a)** Explain Differential amplifier with current mirror load. **07**

(b) Explain need of transistor matching in case of current mirror and discuss different layout techniques. **07**

OR

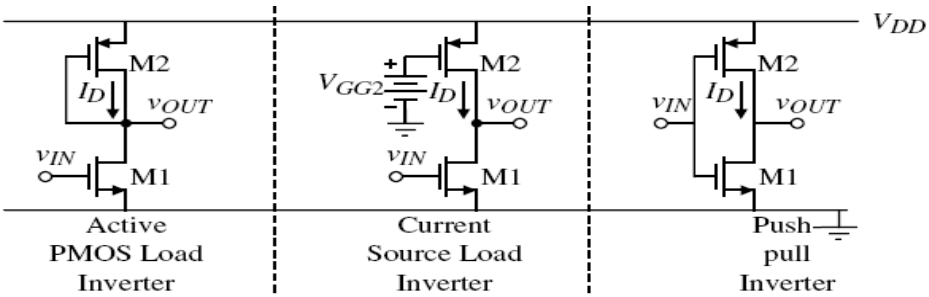
(b) Write short note on MOS device capacitances. **07**

Q.3 **(a)** Explain Miller Compensation for CMOS Op-Amp. **07**

(b) Define the following with respect to Differential Amplifier. **07**
(i) CMRR (ii) ICMR (iii) Output Offset Voltage (iv) PSRR
(v) Differential Mode Voltage (vi) Common Mode Voltage (vii) Slew Rate.

OR

Q.3 **(a)** Find the small-signal voltage gain and the -3dB frequency in Hertz for the active-load inverter, the current source inverter and the push-pull inverter if $W_1 = 2\mu m$, $L_1 = 1\mu m$, $W_2 = 1\mu m$, $L_2 = 1\mu m$ and the dc current is $50\mu A$. Assume that $C_{gd1} = 4fF$, $C_{bd1} = 10fF$, $C_{gd2} = 4fF$, $C_{bd2} = 10fF$ and $C_L = 1pF$. **07**



(b) Discuss in brief Mixed Signal VLSI issues in CMOS Technologies. **07**

Q.4 **(a)** Explain in detail Wilson Current Mirror. **07**

(b) List complete classification of CMOS Op-Amps and explain Two Stage CMOS Op-Amp in brief. **07**

OR

Q.4 **(a)** Explain in brief Slew Rate of the Differential Amplifier. **07**

(b) Explain in brief an intuitive method of small signal analysis. **07**

Q.5 **(a)** Explain in brief second order effects. **07**

(b) Discuss Gilbert cell and voltage headroom. **07**

OR

Q.5 **(a)** Design the currents and W/L values of the current mirror load differential amplifier to satisfy the following specifications: **07**

V_{DD}=-V_{SS}=2.5V, SR ≥ 10V/µs (C_L=5pf), f_{-3db} ≥ 100KHz (C_L=5pf), a small signal gain of 100V/V, -1.5V ≤ ICMR≤ 2.0V, P_{diss} ≤1mW.

(b) Derive $I_{D(Sat)}$ and $I_{D(Lin)}$ for n channel MOSFET. **07**

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Parameter Symbol	Parameter Description	Typical Parameter Value n-Channel	Typical Parameter Value p-Channel	Units
V_{T0}	Threshold voltage (V_{BS} = 0)	0.7 ± 0.15	−0.7 ± 0.15	V
K'	Transconductance parameter (in saturation)	110.0 ± 10%	50.0 ± 10%	µA/V²
γ	Bulk threshold parameter	0.4	0.57	$V^{1/2}$
λ	Channel length modulation parameter	0.04 (L = 1 µm) 0.01 (L = 2 µm)	0.05 (L = 1 µm) 0.01 (L = 2 µm)	V^{-1}
$2\|\phi_F\|$	Surface potential at strong inversion	0.7	0.8	V