

**GUJARAT TECHNOLOGICAL UNIVERSITY**  
**ME – SEMESTER I (NEW) – • EXAMINATION – SUMMER 2016**

**Subject Code: 2715410****Date: 19/05/2016****Subject Name: Advanced Digital Circuit Design****Time: 02:30 pm to 05:00 pm****Total Marks: 70****Instructions:**

1. Attempt all questions.
2. Make suitable assumptions wherever necessary.
3. Figures to the right indicate full marks.

- Q.1** (a) What is static hazard and how to detect static hazard in Multi Level Network **07**  
 (b) Explain in detail different design domain for digital logic design. **07**
- Q.2** (a) What is timing control? Explain (1) Delay-based timing control, (2) Event-based timing control, (3) Level-sensitive timing control. **07**  
 (b) Write a verilog code for 4-bit magnitude comparator. **07**
- OR**
- (b) Write a verilog code for 4-bit ripple counter. **07**
- Q.3** (a) Which are loops statements available in verilog. Explain any two with suitable example **07**  
 (b) Write a verilog code for 4-bit look ahead carry generator. **07**
- OR**
- Q.3** (a) What are the points of difference between task and function **07**  
 (b) Write a verilog code for Bidirectional shift register. **07**
- Q.4** (a) What is Scheduling? Explain (1) As Soon As Possible (ASAP) (2) As Late As Possible (ALAP) and (3) Resource Constrained (List scheduling) Scheduling Algorithms. **07**  
 (b) Write the Verilog code for Sequence detector for detecting "0110" **07**
- OR**
- Q.4** (a) Explain in detail Espresso: A 2-level logic optimizer. **07**  
 (b) Write the Verilog code to implement ALU with given specification. **07**  
     a) There are two data each of 4 bits and two bits control line  
     b) If control is '00' must do addition, '01' subtraction, '10' multiplication, '11' division  
     Assume data is available parallel
- Q.5** (a) Briefly Discuss the points of difference between FPGA, Gate Array, Standard Cell and Full Custom. **07**  
 (b) Briefly Discuss Simulated Annealing Algorithm for Partitioning. **07**
- OR**
- Q.5** (a) Briefly discuss force and release with respect to verilog. **07**  
 (b) Write Verilog code for serial parity detector. **07**

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