Seat No.: _____ Enrolment No._____

GUJARAT TECHNOLOGICAL UNIVERSITY

ME – SEMESTER II (NEW) – • EXAMINATION – SUMMER 2016

Subject Code: 2720314 **Date: 27/05/2016**

Subject Name: ADVANCE VLSI DESIGN

Time:10:30 am to 01:00 pm **Total Marks: 70**

Instructions:

1. **Attempt all questions.**
2. **Make suitable assumptions wherever necessary.**
3. **Figures to the right indicate full marks.**

Q.1	**(a)**	Consider Mealy Finite State Machine (FSM), with one input X and one output Z. The FSM asserts its output Z when it recognize the "1110" input bit sequence. Implement the state diagram for above and write Verilog code for it.	**14**
Q.2	**(a)**	Write Verilog program and test bench for full Adder.	**07**
	(b)	Write a Verilog program for UDP of Negative Edge triggered D flip flop	**07**
		OR	
	(b)	Write Verilog code using dataflow modelling to design BCD to seven segment display assuming common anode display.	**07**
Q.3	**(a)**	Draw the timing diagram observed while simulating the design of x implementation of Iterative architecture in Xilinx ISE that shows all signals observed in simulation window and justifies functionality of the design. State throughput, latency and timing of your design with proper justification.	**07**
	(b)	Implement logic function Y<= A'(B+C) using synchronous set & reset of D flip flop. Write Verilog code and implement diagram.	**07**
		OR	
Q.3	**(a)**	Design 4 bit Ripple carry counter using D flip-flops.	**07**
	(b)	Design 1 to 4 De-multiplexer using if-else statements.	**07**
Q.4	**(a)**	Define function to multiply two 4 bit numbers a and b. The output is an 8 bit value.	**07**
	(b)	Design a clock with time period = 40 and a duty cycle of 25% by using the always and initial statements. The value of clock at time = 0 should be initialized to 0.	**07**
		OR	
Q.4	**(a)**	Write a verilog code for 8 bit universal shift register with shift right, shift left & parallel load capabilities.	**07**
	(b)	Write the Verilog program for 8-bit ALU using Behaviour Modelling.	**07**
Q.5	**(a)**	Write verilog code to design a 4-bit adder using full adder and half adder. Use gate level modelling for half and full adders. Show synthesized output of your design.	**07**
	(b)	Explain Register Balancing for timing in Architecting Speed.	**07**
		OR	
Q.5	**(a)**	Write the Verilog description of the module 3 bit magnitude-comparator. Instantiate the magnitude comparator inside the stimulus module .	**07**
	(b)	Using the wait statement, design a level-sensitive latch that takes clock and d as inputs and q as output. 9 = d whenever clock = 1.	**07**

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