Seat No.:		Enrolment No.	
	ľ	GUJARAT TECHNOLOGICAL UNIVERSITY ME – SEMESTER II (NEW) – • EXAMINATION – SUMMER 2016	
•		Fode: 2720511 Date: 04/06/2016 Date: CMOS CIRCUIT DESIGN - I	
•	10:3 tions	30 am to 01:00 pm Total Marks: 70	
	2. N	Attempt all questions. Make suitable assumptions wherever necessary. Figures to the right indicate full marks.	
Q.1	(a) (b)	Explain the effect of technology scaling on the performance of CMOS inverter. Describe the MOS small signal model.	07 07
Q.2	(a) (b)	Describe the concept of static and dynamic CMOS circuit.  Explain the following circuits (Any two)  (i) Adder Circuits  (ii) Multiplier  (iii) Shifter	07 07
	<b>(b)</b>	<b>OR</b> Explain difference between single ended and differential operation.	07
Q.3	(a) (b)	Describe the basic MOS device physics and general consideration of MOS parameters.  What aspects of the performance of an amplifier are important?	07 07
Q.3	(a) (b)	OR Explain in detail folded cascode amplifier. Explain differential pair with MOS load.	07 07
Q.4	(a) (b)	Explain Gilbert cell. Explain common source stage with diode connected load.  OR	07 07
Q.4	(a) (b)	Explain input output characteristic of CS configuration. Explain basic differential pair and analysis.	07 07
Q.5	(a) (b)	Explain 3 – stage ring oscillator. Explain compensation of two stage op amp and also explain other	07 07

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OR

(a) Describe the two stage op-amp and define slew rate & common mode feedback.(b) Explain I/V characteristic of MOS.

compensation techniques.

Q.5

**07** 

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