Seat No.: _____ Enrolment No._____

# GUJARAT TECHNOLOGICAL UNIVERSITY

**ME – SEMESTER II (NEW) – • EXAMINATION – SUMMER 2016**

**Subject Code: 2722602** **Date: 24/05/2016**

**Subject Name: CMOS Circuit Design - II**

**Time:10:30 am to 01:00 pm** **Total Marks: 70**

**Instructions:**

1. **Attempt all questions.**
2. **Make suitable assumptions wherever necessary.**
3. **Figures to the right indicate full marks.**

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|---|---|---|---|
| **Q.1** | **(a)** | How can we realize resistor using combination of switches and capacitor? Explain working of basic SC integrator circuit (with two switches), discuss the problems associated with its accuracy and draw SC integrator circuit which solves problem of basic SC integrator circuit. | **07** |
| | **(b)** | Draw simple continuous-time domain unity-gain buffer. Convert it to SC unity-gain buffer with just one switch. Draw three switch version of SC unity-gain buffer circuit and compare it with one-switch version. | **07** |
| **Q.2** | **(a)** | How does the op-amp input offset voltage affect the output voltage in temperature independent voltage reference circuit? What are the solutions to solve this problem? Draw the final circuit which has the less effect of op-amp input offset voltage and feasible for implementation in CMOS technology. | **07** |
| | **(b)** | Determine the small-signal output impedance of the bandgap reference circuit shown in Fig. Q:2 (b) and examine its behavior with frequency. | **07** |
| | | **OR** | |
| | **(b)** | What do you understand by jitter? Show that the basic charge pump PLL behaves as low-pass filter for the jitter appearing in input signal and it behaves as high-pass filter for the jitter appearing in VCO signal. | **07** |
| **Q.3** | **(a)** | Draw loop gain characteristics of simple charge pump PLL with and without R in series of C. Discuss the effect of R on stability of the circuit. Derive transfer functions of simple charge pump PLL with R in series of C. | **07** |
| | **(b)** | **1.** Suppose a type I (simple) PLL experiences a frequency step $\omega_x$ at t = 0. Calculate the change in phase error using Laplace transform.<br>**2.** In type I PLL, an external voltage $V_{ex}$ is added to the output of low-pass filter. (a) Determine the phase error and $V_{LPF}$ if the loop is locked and $V_{ex} = V_1$. (b) Suppose $V_{ex}$ steps from $V_1$ to $V_2$ at $t = t_1$. How the PLL will respond? | **07** |
| | | **OR** | |
| **Q.3** | **(a)** | Explain following applications of PLL with diagrams and equations:<br>1. Frequency multiplication and synthesis<br>2. Skew reduction | **07** |
| | **(b)** | What will be the effect of unequal charging and discharging current in basic charge pump PLL on its operation? Explain with necessary waveforms. | **07** |
| **Q.4** | **(a)** | Draw cross section of floating memory element and explain its | **07** |

operation from the point of view of reading, writing and erasing.

**(b)** Sketch a circuit for sensing resistive memory using a concept of DSM and derive expression of $R_{mbit}$. **07**

**OR**

**Q.4** **(a)** What is the need of sense amplifier in reading data from memory cell? Draw circuit diagram of clocked sense amplifier and explain its working. List out various performance parameters of sense amplifier. **07**

**(b)** Draw circuit diagram for a 4-bit NAND flash memory cell. Explain the steps involved in program and read operations performed with this a 4-bit NAND flash memory cell. **07**

**Q.5** **(a)** What are the different performance parameters of voltage comparator? Explain in brief how would you measure each of them with diagrams and waveforms? **07**

**(b)** Briefly discuss following parameters which play a critical role in the overall performance and design of LNA. **07**

1. Noise Figure
2. Input Return Loss
3. Stability

**OR**

**Q.5** **(a)** Define following terms related to DAC: 1. Dynamic range, 2. Quantization noise, 3. Signal-to-noise (SNR) ratio, and 4. Offset error. Derive the general expression for SNR of DAC. **07**

**(b)** Derive noise figure expression for common-gate stage LNA topology. What is/are problem(s) with common-gate stage LNA topology? Suggest possible solution(s). **07**

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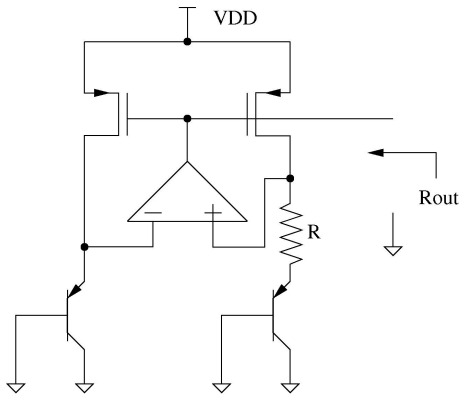


**Figure 1: Q:2 (b)**