Seat No.:	Enrolment No

GUJARAT TECHNOLOGICAL UNIVERSITY

ME - SEMESTER II (NEW) - • EXAMINATION - SUMMER 2016

Subject Code: 2722606 Date: 31/05/2016

Subject Name: Algorithms for VLSI Physical Design Automation

Time: 10:30 am to 01:00 pm **Total Marks: 70**

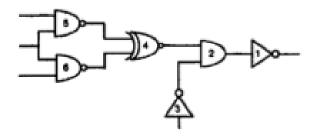
Instructions:

(b)

- 1. Attempt all questions.
- 2. Make suitable assumptions wherever necessary.
- 3. Figures to the right indicate full marks.
- 0.1 Do as Directed: (a)

07

- (i) List Current Layout Styles.
- (ii) Write the equation, which gives relationship between the number of gates and the number of I/O pins and briefly explain it.
- (iii) Discuss with example skewed slicing tree.
- (iv) Define NP-Complete problem
- (v) Discuss Limitations of Lee algorithm for large circuits
- (vi) List general category approaches of Global routing and briefly discuss Global Routing.
- What is the need of Dogleg algorithm?
- The circuit given below is to be partitioned into two sub-circuits. Apply 07 **(b)** Kernighan-Lin heuristics to break the circuit into two equal size partitions, so as to minimize the number of interconnections between partitions. Assume that all gates are of the same size.



List and discuss difficulties in physical design.

Q.2	(a)	List different layout styles and explain Gate-array layout method.	07
	(b)	Discuss Simulated annealing for Floor-Planning.	07
		OR	
	(b)	Explain min-cut placement algorithm along with its limitations.	07
Q.3	(a)	What are the Optimization objectives for placement? Explain various methods to estimate wirelength.	07
	(b)	Compare Kernighan-Lin and Fiduccia-Mattheyses heuristics in reference to circuit partitioning problem?	07
		OR	
Q.3	(a)	Define following terms and briefly explain genetic algorithm. (1) Crossover (2) Mutation (3) Inversion	07
	(b)	Compare Unconstrained left edge algorithm and constrained left edge algorithm in detail.	07
Q.4	(a)	Discuss second algorithm proposed by Yoshimura and Kuh, which achieves longest path minimization through matching techniques on a bipartite graph.	07

07

Q.4	(a) (b)	Discuss Lee algorithm for grid routing in detail. Explain Headlock algorithm for grid routing.	07 07
Q.5	(a)	Explain criteria for channel crossing conversion and discuss conversion algorithm for Global routing.	07
	(b)	Discuss Global routing by maze running	07
		OR	
Q.5	(a)	Explain following in detail:	07
		1. PLA personality 2. PLA Folding	
(b	(b)	List and describe four main graph representations of Floorplans.	07
