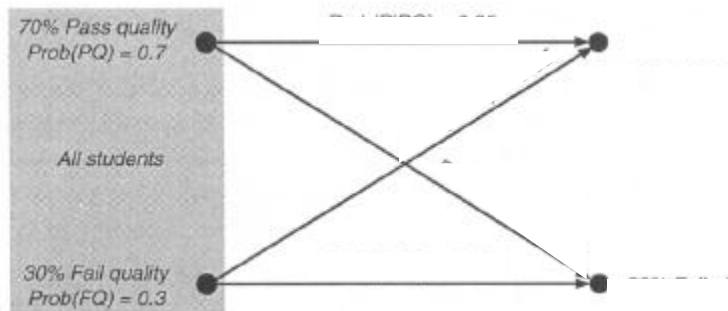# GUJARAT TECHNOLOGICAL UNIVERSITY
ME – SEMESTER II (NEW) – • EXAMINATION – SUMMER 2016

Subject Code: 2724202   **Date: 25/06/2016**
Subject Name: Testing and Verification of VLSI Design
Time:10:30 am to 01:00 pm   **Total Marks: 70**

Instructions:
1. Attempt all questions.
2. Make suitable assumptions wherever necessary.
3. Figures to the right indicate full marks.

Q.1	**(a)**	Explain the Testing philosophy with following example of student pass and fail in the subject of "Testing and Verification". Assume 70% of the students deserve to pass. We will call them "pass quality" students.	**07**

	(b)	Discuss in detail the difference between structural and functional testing?	**07**
Q.2	**(a)**	Can we say verification and testing both are same? Justify your answer with proper discussion.	**07**
	(b)	List down the various VLSI Technology Trends Affecting Testing? Explain any one in detail.	**07**

OR

	(b)	Explain the Permanent and Non-Permanent Fault with example w.r.t Memory Testing.	**07**
Q.3	**(a)**	If you design a product, fabricate and test it, and it fails the test, then what are the various causes of failure? Explain the Role of Testing.	**07**
	(b)	What is the Rule of Ten w.r.t Testing? Explain with suitable example.	**07**

OR

Q.3	**(a)**	List down and explain the various verification strategies?	**07**
	(b)	Explain the Linting Tools? What are the limitation of Linting Toll.	**07**
Q.4	**(a)**	Depending upon the specific purpose accomplishes VLSI testing can be classified into how many types? Discuss each in brief.	**07**
	(b)	List down the various algorithm for fault simulation? Explain any two in detail.	**07**

OR

Q.4	**(a)**	What is Path Delay? Explain the Path Delay Test?	**07**
	(b)	With necessary figure explain the Basic Principal of I_{DDQ} Testing.	**07**
Q.5	**(a)**	Define the following terms.	**07**

    I.   Defect
    II.   Error
   III. Fault

Consider a digital system consisting of two inputs a and b, one output c, and one two-input AND gate. The system is assembled by connecting a wire between the terminal a and the first input of the AND gate. The output of the gate is connected to c. But the connection between b and the gate is incorrectly made b is left unconnected and the second input of the gate is grounded. The

functional
output of this system as implemented, is c =0 instead of the correct output.
Find out Defect, Error and Fault for this system.

	(b)	List down the various types of Fault?	**07**
		Explain the multiple stuck- at fault with necessary figure.	

OR

Q.5	**(a)**	What is BITS? Give Comparison between Online an Offline BITS.	**07**
	(b)	Explain the Following terms	**07**

Reconvergence model
Verification Reuse.
Third Party Model and Hardware moduler.

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