Seat No.: _____ Enrolment No._____

GUJARAT TECHNOLOGICAL UNIVERSITY

ME – SEMESTER II (NEW) – • EXAMINATION – SUMMER 2016

Subject Code: 2724204 **Date: 31/05/2016**

Subject Name: HDL Based Design with Programmable Logic

Time:10:30 am to 01:00 pm **Total Marks: 70**

Instructions:

1. **Attempt all questions.**
2. **Make suitable assumptions wherever necessary.**
3. **Figures to the right indicate full marks.**

Q. 1 1 Which one of the following is not the fundamental VHDL unit? 14

A. ENTITY
B. ARCHITECTURE
C. LIBRARY
D. FUNCTION

2 Identify the concurrent statement among the following VHDL constructs.

A. PROCESS
B. LOOP
C. CASE
D. BLOCK

3 The empty sensitivity list in the process statement is identical to _____.

A. WAIT ON
B. WAIT FOR
C. WAIT UNTILL
D. WAIT

4 In VHDL, the mode of a port does not define

A. AN INPUT
B. AN OUTPUT
C. AN INPUT AND OUTPUT
D. THE TYPE OF THE BIT

5 Which of the following is having fine grained architecture?

A. FPGA
B. CPLD
C. ROM
D. PAL

6 Which of the following does not belongs to Design Quality?

A. RELIABILITY
B. UPGRADIBILITY
C. GATE LEVEL DESIGN
D. MANUFACTURIBILITY

7 Which one of the following is not an EDA tool?

A. XILINX ISE
B. ALTERA QUARTUS
C. LEONARDO SPECTRUM
D. MATLAB

8 For designing higher end DSP processor, which of the following design methodology will be most suitable?

A. FULL CUSTOM
B. STANDARD CELL
C. GATE ARRAY
D. FPGA

9 If the declarative part in the architecture of a half adder is as below

```
component XOR2
        port (X,Y:in BIT;z: out BIT);
end component
```

component AND2
port (L,M:in BIT;z:out BIT);
end component
Then what kind of architecture is it?

A. BEHAVOURIAL
B. STRUCTURAL
C. DATAFLOW
D. NONE OF THESE

10 Which statement is used to terminate the current loop iteration and proceed on the next iteration

A. NEXT
B. EXIT
C. BOTH OF THESE
D. NONE OF THESE

11 Which of these is a valid identifier in VHDL?

A. _c5
B. 5c
C. c_5
D. process

12 The complex programmable logic device (CPLD) contains several PLD blocks and:

A. field-programmable switches
B. AND/OR arrays
C. A global interconnection matrix
D. A language compiler

13 The difference between a PLA and a PAL is:

A. the PLA has a programmable OR plane and a programmable AND plane, while the PAL only has a programmable AND plane
B. the PAL has a programmable OR plane and a programmable AND plane, while the PLA only has a programmable AND plane
C. the PAL has more possible product terms than the PLA
D. PALs and PLAs are the same thing

14 FPGA device XC3S500E-4 has logic density of _____ logic gates.

A. 500
B. 50,000
C. 50K
D. None of the above

Q.2 (a) 1. What are the different levels of abstraction in VLSI design? Discuss pros and cons of each one of them. 04

2. Identify the operation of the below given VHDL code. 03

```
ARCHITECTURE dff OF dff IS
BEGIN
   b1: BLOCK (clk'EVENT AND clk='1')
   BEGIN
      q <= GUARDED '0' WHEN rst='1' ELSE d;
   END BLOCK b1;
END dff;
```

(b) Explain, what functionality following VHDL code does implement? Use diagrams wherever needed. 07

```
ENTITY system IS
        PORT (  in_data : IN BIT_VECTOR ( 3 DOWNTO 0 );
                out_data : OUT BIT_VECTOR ( 3 DOWNTO 0 );
                in_ready, out_receivedt : IN BIT;
                in_received, out_ready : OUT BIT );
END system;
```

```
ARCHITECTURE behavioral OF system IS
        SIGNAL buffer_full, buffer_picked : BIT := '0';
        SIGNAL word_buffer : BIT_VECTOR ( 15 DOWNTO 0);
BEGIN
        a_talk: PROCESS ( )
                VARIABLE count : INTEGER RANGE 0 TO 4 := 0;
        BEGIN
                WAIT UNTIL in_ready = '1';
                count := count + 1;
                CASE count IS
                        WHEN 0 => NULL;
                        WHEN 1 => word_buffer (   3 DOWNTO   0 ) <= in_data;
                        WHEN 2 => word_buffer (   7 DOWNTO   4 ) <= in_data;
                        WHEN 3 => word_buffer ( 11 DOWNTO   8 ) <= in_data;
                        WHEN 4 => word_buffer ( 15 DOWNTO 12 ) <= in_data;
                                buffer_full <= '1';
                                WAIT UNTIL buffer_picked = '1';
                                buffer_full <= '0';
                                count := '0';
                END CASE;
                in_received <= '1';
                WAIT UNTIL in_ready = '0';
                in_received <= '0';
        END PROCESS a_talk;

        b_talk: PROCESS ( )
        BEGIN
                IF buffer_full = '0' THEN WAIT UNTIL buffer_full = '1'; END IF;
                out_data <= word_buffer;
                buffer_picked <= '1';
                WAIT UNTIL buffer_full = '0';
                buffer_picked <= '0';
                out_ready <= '1';
                WAIT UNTIL out_received = '1';
                out_ready <= '0';
        END PROCESS b_talk;
END behavioral;
```

OR

(b) Using several instances of the T flip-flop and simple gates supplied below, which are available in the WORK library in dataflow architecture. D**esign** and **implement** a 4-bit binary up counter in VHDL using the code template provided. 07

The counter should have an asynchronous RESET. The counter keeps counting when the active high input signal START is asserted. The counter should generate an active high DONE signal when a total of 10 clock cycles are counted.

The entity declarations for the components are given below.

```
ENTITY  t_ff    IS  PORT (  t, clk, rst : IN BIT; q, qb : OUT BIT ); END t_ff;
ENTITY  and2  IS  PORT (  i1, i2 : IN BIT; o1 : OUT BIT ); END and2;
ENTITY  and3  IS  PORT (  i1, i2, i3 : IN BIT; o1 : OUT BIT ); END and3;
ENTITY  and4  IS  PORT (  i1, i2, i3, i4 : IN BIT; o1 : OUT BIT ); END and4;
```

```
ENTITY  or2    IS  PORT (  i1, i2 : IN BIT; o1 : OUT BIT ); END or2;
ENTITY  or3    IS  PORT (  i1, i2, i3 : IN BIT; o1 : OUT BIT ); END or3;
ENTITY  or4    IS  PORT (  i1, i2, i3, i4 : IN BIT; o1 : OUT BIT ); END or4;
ENTITY  xor2   IS  PORT (  i1, i2 : IN BIT; o1 : OUT BIT ); END xor2;
ENTITY  not1   IS  PORT (  i1, i2 : IN BIT; o1 : OUT BIT ); END not1;
```

CODE TEMPLATE

```
ENTITY  counter4   IS
        PORT (  reset, start, clk : IN BIT; done : OUT BIT );
END counter4;

ARCHITECTURE structural OF counter 4 IS
    COMPONENT ___________ IS
            PORT ( _______________: IN BIT; _________ : OUT BIT );
    END COMPONENT;
    COMPONENT ___________ IS
            PORT ( _______________: IN BIT; _________ : OUT BIT );
    END COMPONENT;
                .
            .
            .
    DECLARE YOUR SIGNALS HERE
BEGIN
    INST0: _____________ PORT MAP ( ________________________________ );
    INST1: _____________ PORT MAP ( ________________________________ );
                .
            .
            .
END structure;
```

Q.3 (a) Realize following functions using PLA. What is the total number of programming links required? 07

$$F_1 = \sum(0,2,4,6)$$
$$F_2 = \Sigma(1,3,5,7)$$
$$F_3 = \sum(0,2,5,7)$$
$$F_4 = \sum(4,6,1,3)$$

(b) Draw and explain the basic architecture of an FPGA. Enlist the features available in current generation of FPGA. 07

OR

Q.3 (a) Implement following Boolean equations using PAL. How many total programmable links required? How many of them are fused out to implement the given digital logic? 07

$$P(A,B,C,D) = \sum m(2,12,13)$$
$$Q(A,B,C,D) = \prod M(0,1,2,3,4,5,6)$$
$$R(A,B,C,D) = \prod M(1,9,12,13,14)$$
$$S(A,B,C,D) = \sum m(1,2,8,12,13)$$

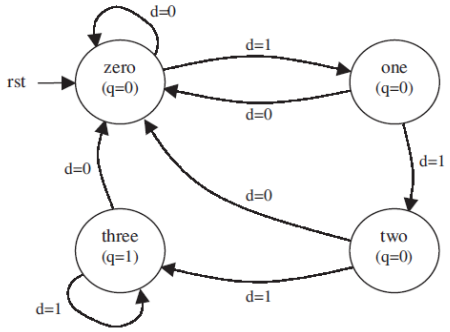
(b) Draw and explain the basic building block of any CPLD device. 07

Q.4 (a) For the state machine given below, 07

(i) Identify whether is it a Melay or a Moore Machine?

(ii) Write the VHDL description

(iii) Draw the output waveform w.r.t. the clock if the input sequence is 011111100.



(b) 1. Explain following terms in reference to Digital Design. 03

I. High Level Synthesis

II. RTL Synthesis

III. Gate Level Synthesis

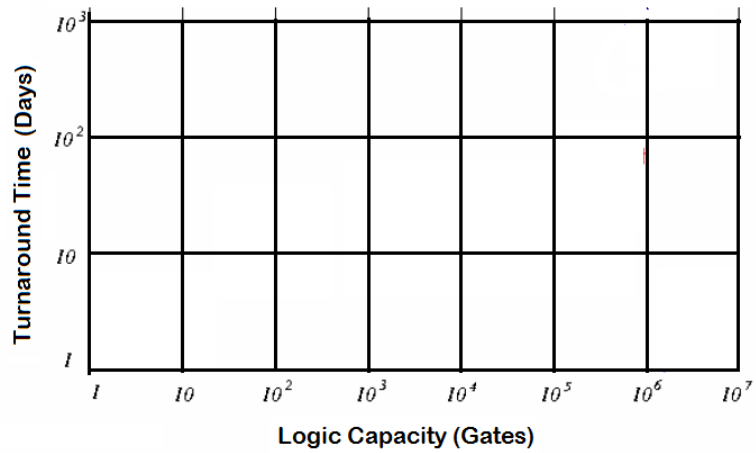
2. Mention various verification techniques used at different VLSI design abstraction levels. Describe static timing analysis and its objective in brief. 04

OR

Q.4 (a) Define Event-Driven Simulator and Cycle-Based Simulators. What are the pros and cons of the two? Describe the operation of Event Based Simulator with suitable example. 07

(b) 1. Differentiate between 'EVENT' and 'TRANSACTION' with the help of suitable example. 02

2. Map various logic design styles (SSI, SPLD, CPLD, FPGA, Standard-cell, Full Custom) on the given plot of Design Time → Logic Capacity 05



Q.5 (a) 1. Discuss the use of following Verilog constructs/operator. 04

a) Module

b) Wire

c) Reg

d) Assign

2. The use of explicit and implicit wait statement is presented below. 03

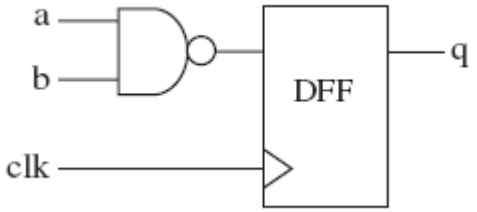
```
process (A,B)
begin
    C <= A and B;
end process;
```

```
process
begin
    wait on A, B;
    C <= A and B;
end process;
```

```
process
begin
    C <= A and B;
    wait on A, B;
end process;
```

Assume that all processes are initialized before simulation, which means that they are already running until the first wait condition is met. Also assume std_logic data type for each of the signal above.
Given this fact, what is the value on C at simulation time zero in each case?

(b) Write the VHDL Test Bench to test the functionality of the below given digital circuit. 07



OR

Q.5 (a) 1. Discuss various LOOP structures available in VHDL. Also mention 05
   a) How a loop can skip iteration?
   b) How the control can exit from the loop?
2. What are the salient differences in Verilog against VHDL? Mention any four. 02

(b) Draw the RTL of below given VHDL code and write equivalent Verilog code for the same. 07

```
ENTITY  sample   IS
            PORT (  x, y : IN BIT_VECTOR (1 downto 0);
                    c_in : IN BIT;
                    sum, c_out : OUT BIT);
END sample;
ARCHITECTURE rtl OF sample IS
        COMPONENT add IS
                PORT ( a, b : IN BIT; s, c : OUT BIT );
        END COMPONENT;
        SIGNAL p,q,r,s : BIT := '0';
BEGIN
        add0 : add port map (x(0), y(0), p, q);
        add1 : add port map (x(1), y(1), r, s);
        sum <= p XOR r;
        c_out <= q AND s;
END rtl;
```

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