Seat No.:	Enrolment No.
Seat NO	Emoment No.

## **GUJARAT TECHNOLOGICAL UNIVERSITY**

ME – SEMESTER II (NEW) – • EXAMINATION – SUMMER 2016

•		Code: 2724207 Date: 31/05/	
•	:10:	Name: HARDWARE SOFTWARE CO-DESIGN 30 am to 01:00 pm Total Marks	: 70
	1. 2.	Attempt all questions.  Make suitable assumptions wherever necessary.  Figures to the right indicate full marks.	
Q.1	(a) (b)	•	07 07
Q.2	(a) (b)		07 07
	<b>(b</b> )		07
Q.3	(a) (b)	Discuss partitioning issues.	07 07
0.1	(	OR	07
Q.3	(a) (b)		07 07
Q.4	(a)	Explain Accuracy Vs Speed in terms of estimation issues. Also explain fidelity.	07
	<b>(b</b> )	) Compare VHDL and VERILOG as a specification language.	07
0.4	(6)	OR  What are the differences between state charts and spee aborts? Explain any	07
Q.4	(a)	What are the differences between state charts and spec charts? Explain any one.	U/
	<b>(b</b> )	How state machine model helps to design three floor elevators? Discuss it.	07
Q.5	(a)	Explain RISC and CISC & compare it.	07
	<b>(b</b> )	Discuss Queuing models.	07
		OR	
Q.5	(a)		07
		<ol> <li>Hardware Software Co-Design 2. Modeling 3. Validation 4. Partitioning</li> <li>Scheduling 6. Synthesis 7. Allocation</li> </ol>	
	<b>(b</b> )	Write a note on SDL.	07