Seat No.: _____ Enrolment No._____

GUJARAT TECHNOLOGICAL UNIVERSITY

ME – SEMESTER II (NEW) – • EXAMINATION – SUMMER 2016

Subject Code: 2724209 **Date: 27/05/2016**

Subject Name: VLSI Signal Processing

Time:10:30 am to 01:00 pm **Total Marks: 70**

Instructions:

1. **Attempt all questions.**
2. **Make suitable assumptions wherever necessary.**
3. **Figures to the right indicate full marks.**

Q.1 **(a)** 1. The longest combinational path in the digital design is referred as _____. **07**

2. The cutset is defined as …….
3. LPM and MCM algorithms are used for computing _____.
4. In below given precedence constraint graph, what does $\rightarrow$ and $\Rightarrow$ represent?

$$A_0 \rightarrow B_0 \Rightarrow A_1 \rightarrow B_1 \Rightarrow A_2 \rightarrow B_2 \Rightarrow A_3 \rightarrow ...$$

5. What do you mean by Critical Loop?
6. Which algorithms are used for computing iteration bound?
7. The iteration bound of a DSP algorithm is 5 ns. What does it mean?

(b) Write a short note on various DSP Algorithm representation methods. **07**

Q.2 **(a)** Define the feed-forward cutset and critical path. In signal flow graph given in *Figure 1*, identify the critical path and reduce it to 1 u.t. by inserting extra delays in the critical path. How many total numbers of extra delays are required for reducing the critical path to 1 u.t.? **07**

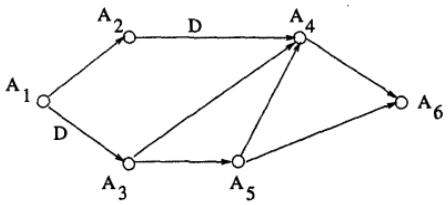

Figure 1

(b) Consider the 3-tap FIR filter given in *Figure 2* and its fine-grained version in *Figure 3*. The computation time of each execution block is mentioned in the Figures. Consider the capacitance of the multiplier in reference to capacitance of the adder as, **07**

$Cmul = 5*Cadder$, $Cm_1 = 3*Cadder$, $Cm_2 = 2*Cadder$ (Where C represents the capacitance).

Assume the device threshold voltage is 0.6 V. Also assume that non-pipelined filter to be operated at the supply voltage of 5 V.

1. What should be the supply voltage of the pipelined filter if the clock period needs to be kept unchanged?
2. What is the power consumption of the pipelined filter as a percentage of the original filter?

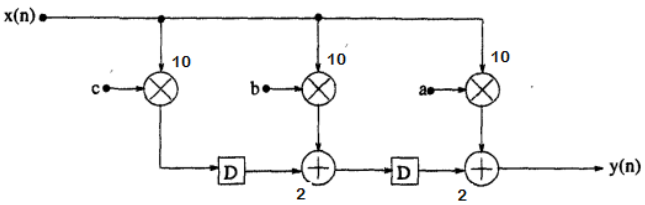

Figure 2 : Data-broadcast structure of the 3-tap FIR filter

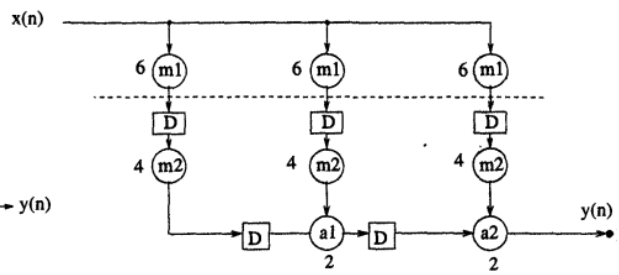

Figure 3 : Fine-grain Pipelining of the 3-tap FIR filter

OR

(b) Compute iteration bound of the system, represented by DFG given in *Figure 4* using LPM technique. **07**

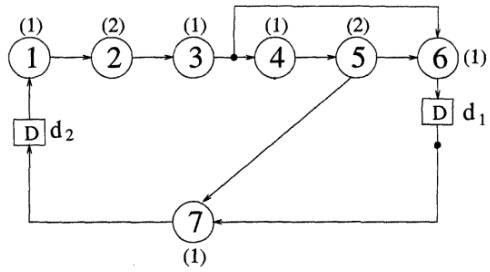

Figure 4

Q.3 **(a)** List all the power reduction techniques and discuss any two of them in detail. **07**

(b) Unfold the DFG given in *Figure 5* with unfolding factor equal to 2. Also compute the iteration bound and minimum sample period for both, given DFG as well as unfolded DFG. **07**

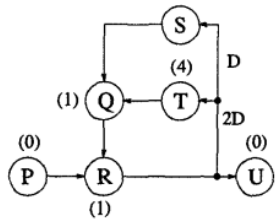

Figure 5 : Given DFG

OR

Q.3 **(a)** What is retiming? What are the applications of retiming? What are the techniques of retiming? **07**

Derive the retimed DFG for the DFG given in *Figure 6* using cutset retiming technique with k=1.

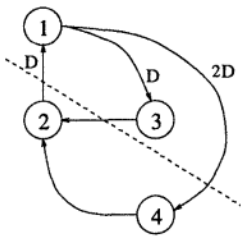

Figure 6 : Given DFG

(b) Prove that Unfolding preserves the number of delays in a DFG. **07**

Q.4 **(a)** What is the need for systolic architecture design? Discuss systolic architecture design in detail. **07**

(b) What is folding? What are its applications in VLSI Signal Processing? Implement the DSP program $y(n) = a(n) + b(n) + c(n)$ with minimum number of Adders. **07**

OR

Q.4 **(a)** Discuss Cook-Toom Algorithm for fast convolution. **07**

(b) What is the numerical strength reduction? Explain it using Sub-expression Elimination method with suitable example. **07**

Q.5 **(a)** What are the architectural features required in a DSP Processor? Justify with explanation. **07**

(b) List and discuss common DSP algorithms and their applications. **07**

OR

Q.5 **(a)** In reference to redundant number representation, explain following terms. **07**

1. Non-Redundant
2. Redundant
3. Minimally Redundant
4. Maximally Redundant
5. Over Redundant
6. Redundancy factor (ρ)
7. On-line Arithmetic

(b) Discuss following in reference to implementation of DSP algorithms in Software or VLSI HW. **07**

1. Scaling
2. Round-off Noise

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