Seat No.: _____ Enrolment No._____

# GUJARAT TECHNOLOGICAL UNIVERSITY

**ME – SEMESTER II (NEW) – • EXAMINATION – SUMMER 2016**

**Subject Code: 2725406 Date: 27/05/2016**

**Subject Name: Embedded and VLSI Signal Processing**

**Time:10:30 am to 01:00 pm Total Marks: 70**

**Instructions:**

1. **Attempt all questions.**
2. **Make suitable assumptions wherever necessary.**
3. **Figures to the right indicate full marks.**

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|---|---|---|---|
| **Q.1** | **(a)** | Discuss general architecture of FPGA also Compare semi-custom and full custom VLSI design style | **07** |
| | **(b)** | Briefly discuss the Static and Dynamic characteristics of ADC (Analog to Digital Convertor) with suitable transfer curve. | **07** |
| **Q.2** | **(a)** | Draw CMOS inverter circuit. Mention the operating regions for different critical voltages in VTC also derive critical voltage points $V_{OH}$, $V_{OL}$ and $V_{IL}$ | **07** |
| | **(b)** | Define impulse response of LTI system. Explain how from the impulse response the frequency response of the LTI system can be determined. | **07** |
| | | **OR** | |
| | **(b)** | Write VHDL code for 16:1 data selector circuit using structural modeling use 8:1 Multiplexer as a component. | **07** |
| **Q.3** | **(a)** | Draw transistor level implementation of CMOS 6-T SRAM also briefly discuss its read write operation | **07** |
| | **(b)** | Explain the fabrication steps of nMOS transistor with necessary diagrams | **07** |
| | | **OR** | |
| **Q.3** | **(a)** | Explain sampling and reconstruction theorem with aliasing effect. | **07** |
| | **(b)** | Explain data types used in VHDL. List all possible level that can be assigned to std_ulogic data type. | **07** |
| **Q.4** | **(a)** | What do you understand by delta – delay? Also explain Inertial delay model and transport delay model with suitable waveforms | **07** |
| | **(b)** | Write a VHDL code for 8 bit Right shift Register using if else statement | **07** |
| | | **OR** | |
| **Q.4** | **(a)** | List the different abstraction level of digital circuit design. Also give difference between top-down and bottom- up methodologies used for circuit design. | **07** |
| | **(b)** | Draw two input CMOS NOR gate and derive the necessary equations for critical voltage and also realize the given Boolean function using CMOS TG (Transmission Gates) F = AB + A'C' + AB'C | **07** |
| **Q.5** | **(a)** | Describe the advantages and disadvantages of FIR filter over IIR filter | **07** |
| | **(b)** | Draw transistor level schematic and stick diagram layout of the given Boolean function Z= {A.(D+E)+B.C}' | **07** |
| | | **OR** | |
| **Q.5** | **(a)** | Draw CMOS clocked JK latch and explain its operating modes of the transistor | **07** |
| | **(b)** | Define ACF (Auto-Correlation Function) of a sequence; explain ACF main properties and relation with the Power Spectral Density of the sequence. | **07** |

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