Seat No.: _____ Enrolment No._____

GUJARAT TECHNOLOGICAL UNIVERSITY

ME – SEMESTER IV (NEW) – • EXAMINATION – SUMMER 2016

Subject Code: 2744202 Date:04/05/2016

Subject Name: Power Efficient VLSI Design

Time:10:30 am to 01:00 pm Total Marks: 70

Instructions:

1. **Attempt all questions.**
2. **Make suitable assumptions wherever necessary.**
3. **Figures to the right indicate full marks.**

Q.1	**(a)**	Explain in detail source of power dissipation in CMOS.	**07**
	(b)	Why n-well CMOS Process? Why not p-well CMOS Process?	**07**
Q.2	**(a)**	Explain Self-Reverse Biasing.	**07**
	(b)	Explain low dynamic power techniques.	**07**
		OR	
	(b)	Discuss Tolerable Skew v/s Zero Skew.	**07**
Q.3	**(a)**	Derive mathematical expression to avoid negative tolerable skew and positive tolerable skew.	**07**
	(b)	Illustrate the effect of wire widening and intermediate buffer insertion on delay reduction using mathematical expression.	**07**
		OR	
Q.3	**(a)**	Discuss data retention power sources for DRAM and SRAM.	**07**
	(b)	Discuss Monte Carlo Simulation Technique for power estimation with necessary expressions.	**07**
Q.4	**(a)**	What is Glitch? Discuss various techniques used for glitch reduction in low power design.	**07**
	(b)	Explain Power and Performance Management.	**07**
		OR	
Q.4	**(a)**	Discuss in brief the effect of transistor and gate sizing for Power Efficient VLSI Design.	**07**
	(b)	Explain algorithm level analysis and optimization.	**07**
Q.5	**(a)**	Discuss architectural level estimation and synthesis.	**07**
	(b)	Compare SPICE simulation based power simulation v/s statistical based power estimation techniques.	**07**
		OR	
Q.5	**(a)**	Discuss the effect of process variation on the performance of clock distribution network.	**07**
	(b)	Explain Multi -V_T Technique.	**07**

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