Seat No.: _____ Enrolment No._____

GUJARAT TECHNOLOGICAL UNIVERSITY

ME – SEMESTER IV (NEW) – • EXAMINATION – SUMMER 2016

Subject Code: 2745402 **Date:04/05/2016**

Subject Name: Cortex-M4 Processor Architecture and Programming

Time:10:30 am to 01:00 pm **Total Marks: 70**

Instructions:

1. **Attempt all questions.**
2. **Make suitable assumptions wherever necessary.**
3. **Figures to the right indicate full marks.**

Q.1	**(a)**	Explain in Detail Cortex-M family Processor Architecture.	**07**
	(b)	What is SYSTICK timer? Explain each bit in SYSTICK control and status register?	**07**
Q.2	**(a)**	What facilities NVIC provides?	**07**
	(b)	What are the registers available in CORTEX M4?	**07**
		OR	
	(b)	What is Bus Interface Unit? Explain types of Bus Interface Unit?	**07**
Q.3	**(a)**	What is the significance of Pseudo instructions?	**07**
	(b)	What is the difference between THUMB 1 and THUMB 2 Architecture?	**07**
		OR	
Q.3	**(a)**	How branch instructions are executed in CORTEX M4?	**07**
	(b)	Explain with example: 1)DMB 2)DSB 3)ISB	**07**
Q.4	**(a)**	What are CMSIS usage and benefits?	**07**
	(b)	List the CMSIS intrinsic instruction and explain any two in detail.	**07**
		OR	
Q.4	**(a)**	Explain with block diagram Cortex Microcontroller Software Interface standard (CMSIS).	**07**
	(b)	Discuss about CMSIS Register Core in detail.	**07**
Q.5	**(a)**	Explain with diagram Memory map in cortex.	**07**
	(b)	Explain in Detail Memory Bit Band operation.	**07**
		OR	
Q.5	**(a)**	Explain in detail Lazy stacking in Floating Point Unit.	**07**
	(b)	Explain following terms: 1) AHB Trace Macro cell 2) DEMCR.	**07**

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