Seat No.: _____ Enrolment No._____

GUJARAT TECHNOLOGICAL UNIVERSITY

ME – SEMESTER I (NEW) – • EXAMINATION – SUMMER 2016

Subject Code: 3715201 **Date:17/05/2016**

Subject Name: Advanced Computer Architecture

Time:02:30 pm to 05:00 pm **Total Marks: 70**

Instructions:

1. **Attempt all questions.**
2. **Make suitable assumptions wherever necessary.**
3. **Figures to the right indicate full marks.**

Q.1 **(a)** - What is a stored program computer? Explain the concept of stored program with block diagram? **07**

- Suppose a system has four register A, B, C and D. Value of variable X = 31 and Y = 15. Then calculate (X + Y) * (X - Y)

Write assembly code to implement above formula and explain benefits of stored program concept in implementing above formula. Register C Shall contain final result

(b) - What do you mean by byte order in computer architecture? Explain the difference between ñLittle Endianò and ñBig Endianò byte order scheme with example. **07**

Q.2 **(a)** - A computer system uses direct mapped cache mapping scheme. The Main memory size of this computer is 2^32 words and has cache of 1024 blocks. Each of the cache block contains 32 words then - **07**

a) Calculate the number of blocks of main memory.

b) what is size of tag, block and word field?

c) Calculate cache block number to which the memory reference (000063FA) base 16 will be mapped?

(b) - The code on a CISC machine of product 9 * 12 might look as bellow: **07**

```
mov ax, 12
mov bx, 9
mul bx, ax
```

Convert this assembly code to equivalent minimalistic RICS ISA which does not have *mul* (multiplication) instruction. You can use *jmp* instruction in RICS code.

OR

	(b)	Describe major components of Von-Neumann architecture in detail using block diagram.	**07**
Q.3	**(a)**	- Explain with block diagram, how TLB (Translation look-aside buffer) helps to manage the access of pages from memory under Virtual Memory Management Scheme.	**07**
	(b)	- In instruction pipelining what is pipeline hazards - explain any ONE kind of pipeline hazards with suitable example.	**07**

OR

Q.3	**(a)**	- Define System-on-Chip(SoC) architecture and its properties. - Discuss how SoC is different from Multi-Core systems from architecture point of view.	**07**
	(b)	- Explain in detail with block diagram - Components of Memory Hierarchy in modern computing system and its importance. - Discuss memory bottleneck issue and how it managed through Hierarchical Memory Organization.	**07**
Q.4	**(a)**	- A word addressable digital computer has memory unit with 24 bits per word. The instruction set consists of 150 different operations. All instructions have an operation code part(opcode) and an address part (allowing for only one address). Each instruction is stored in one word of memory. a) How many bits are needed for the opcode? b) How many bits are left for the address part of the instruction? c) What is the maximum allowable size for memory? d) What is the largest unsigned binary number that can be accommodated in one word of memory?	**07**

(b) - Discuss in detail **07**

i) Multiprocessor system architecture vs multi-core system architecture

ii) Vector machines

OR

Q.4 **(a)** - What is vector processors? Why vector processors are important in Scientific Computing? Write down 4(Four) properties of vector processor and their benefits. **07**

(b) - What is super scalar processor ? How is it related to ILP ? **07**

Explain with example - how ILP can be limited by

i) True data dependency

ii) Resource conflicts.

Q.5 **(a)** - Given byte-addressable memory of 2048 bytes consisting of several 64 Byte * 8 RAM chips - then **07**

i) Calculate Number of address bit required

ii) Give block diagram of address with chip select and word select field.

(b) - Explain in detail fetch-decode-execute cycle. Discuss the sate of various registers during each of the steps. **07**

OR

Q.5 **(a)** - What do you mean by data locality of reference ? **07**

- Explain in detail following terms with suitable code snippet /example -

i) Temporal locality

ii) Spatial locality

iii) Sequential locality

(b) - Define 5(Five) difference between RICS and CISC architecture. **07**

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