Seat No.: _____ Enrolment No._____

GUJARAT TECHNOLOGICAL UNIVERSITY

ME – SEMESTER I (NEW) – • EXAMINATION – SUMMER 2016

Subject Code: 3715204 **Date:20/05/2016**

Subject Name: Digital VLSI Design & Verification-I Frontend

Time:02:30 pm to 05:00 pm **Total Marks: 70**

Instructions:

1. **Attempt all questions.**
2. **Make suitable assumptions wherever necessary.**
3. **Figures to the right indicate full marks.**

Q.1	**(a)**	Compare BJT & MOSFET in detail.	**07**
	(b)	Write short note on FPGA Tools.	**07**
Q.2	**(a)**	Explain various SoC Design cores in detail.	**07**
	(b)	Explain importance of RTL Synthesis tool in detail.	**07**
		OR	
	(b)	Explain Backend design flow in detail.	**07**
Q.3	**(a)**	Explain various VLSI Design styles in detail.	**07**
	(b)	Explain Microscopic issues as design challenges.	**07**
		OR	
Q.3	**(a)**	Explain Macroscopic issues as design challenges.	**07**
	(b)	Write short note on VLSI Design Hierarchy.	**07**
Q.4	**(a)**	Write short note on AMBA AX14 Protocol in detail.	**07**
	(b)	Explain DRC & ERC with an example.	**07**
		OR	
Q.4	**(a)**	Write short note on FSM.	**07**
	(b)	Explain RTL Design for sequential & combinational circuits.	**07**
Q.5	**(a)**	Write short note on CAD Tools.	**07**
	(b)	Explain verification process using Verilog.	**07**
		OR	
Q.5	**(a)**	Explain BJT Structure and its principle of operation.	**07**
	(b)	Compare VHDL & Verilog for design & synthesis.	**07**

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