Seat No.: _____ Enrolment No._____

GUJARAT TECHNOLOGICAL UNIVERSITY

ME – SEMESTER II (NEW) – • EXAMINATION – SUMMER 2016

Subject Code: 3725203 **Date: 27/05/2016**

Subject Name: Digital VLSI Design - II Backend

Time:10:30 am to 01:00 pm **Total Marks: 70**

Instructions:

1. **Attempt all questions.**
2. **Make suitable assumptions wherever necessary.**
3. **Figures to the right indicate full marks.**

Q.1 **(a)** Compare ASIC and FPGA Designs. **07**

(b) Write Inputs and Outputs at each and every stage of Physical Design **07**

Q.2 **(a)** Draw and Explain Y-Chart for Design in Detail. **07**

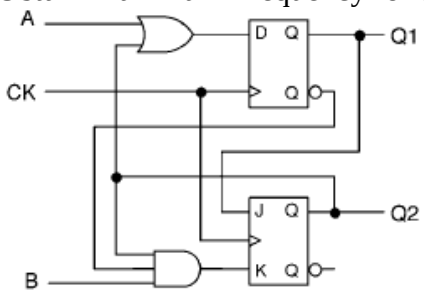
(b) What is Verification? Explain different approaches for Functional Verification? **07**

OR

(b) What is Synthesis and Simulation mismatch? Explain using following examples **07**
a. Incomplete Sensitivity List
b. Latch Inference.

Q.3 **(a)** How to get improved Macro Placement? **07**

(b) Obtain Maximum Frequency for the following circuit. **07**



	t_P	t_{su}
D Flip-Flop:	20 ns	5 ns
JK Flip-Fllp:	25 ns	10 ns
AND Gate:	12 ns	
OR Gate:	10 ns	

OR

Q.3 **(a)** Explain 1-D and 2-D compaction with diagrams **07**

(b) Explain place_opt with area recovery and congestion option? **07**

Q.4 **(a)** What are basic components of IO cells with classification of IO cells? **07**

(b) Explain different paths you analyze while performing Static Timing Analysis **07**

OR

Q.4 **(a)** Explain On-chip Variation and CRPR (Clock Reconvergence Pessimism Removal). **07**

(b) Design Status before Clock Tree Synthesis. Mention Clock Tree Synthesis Goals. **07**

Q.5 **(a)** Design Status before Routing. Draw and Explain General flow for Routing. **07**

(b) What is crosstalk? Why we have crosstalk issue? What kinds of problems are induced due to crosstalk? **07**

OR

Q.5 **(a)** Explain Global Routing in Detail. **07**

(b) Explain what signal integrity issues are and Design integrity issues? How to prevent them. **07**

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