Seat No.: _____ Enrolment No._____

GUJARAT TECHNOLOGICAL UNIVERSITY

ME – SEMESTER II (NEW) – • EXAMINATION – SUMMER 2016

Subject Code: 3725204 Date: 31/05/2016

Subject Name: Designing with Modeling & FPGA's

Time:10:30 am to 01:00 pm Total Marks: 70

Instructions:

1. **Attempt all questions.**
2. **Make suitable assumptions wherever necessary.**
3. **Figures to the right indicate full marks.**

Q.1	**(a)**	Explain differential pair with MOS load.	**07**
	(b)	Explain I/V characteristic of MOS.	**07**
Q.2	**(a)**	Describe the MOS small signal model.	**07**
	(b)	What aspects of the performance of an amplifier are important?	**07**
		OR	
	(b)	Describe the basic MOS device physics and general consideration of MOS parameters	**07**
Q.3	**(a)**	What is Jitter? Explain foe PLL	**07**
	(b)	Explain switched capacitor integrator?	**07**
		OR	
Q.3	**(a)**	Explain basic differential pair and analysis.	**07**
	(b)	What is clock feed through ? and what in delay locked loops PLL	**07**
Q.4	**(a)**	What are types of feedback topologies? Briefly explain with diagram	**07**
	(b)	Explain the miller theorem and also discuss the significance.	**07**
		OR	
Q.4	**(a)**	Explain Gilbert cell.	**07**
	(b)	Describe the basic MOS device physics and general consideration of MOS parameters	**07**
Q.5	**(a)**	Explain common source stage with diode connected load.	**07**
	(b)	Explain in short (i) Threshold voltage (ii) Noise margin. (iii) Circuit design levels.	**07**
		OR	
Q.5	**(a)**	Explain cascode current mirrors.	**07**
	(b)	Write short note on any two 1. Binary weighted resister 2. R-2R Ladder 3. Multiplier DAC 4. Non-Multiplier DAC	**07**

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