Seat No.: _____ Enrolment No._____

GUJARAT TECHNOLOGICAL UNIVERSITY

ME – SEMESTER II (NEW) – • EXAMINATION – SUMMER 2016

Subject Code: 3735205 **Date: 02/06/2016**

Subject Name: System on Chip Architecture

Time:10:30 am to 01:00 pm **Total Marks: 70**

Instructions:

1. **Attempt all questions.**
2. **Make suitable assumptions wherever necessary.**
3. **Figures to the right indicate full marks.**

Q.1	**(a)**	Draw Architectural Block Diagram of PSoC 5LP Programmable embedded SoC. Briefly explain its major components.	**07**
	(b)	Compare the SoC platforms from Tilera, TI and Feescale.	**07**
Q.2	**(a)**	Explain the benefits of AXI4 bus when doing system development using FPGA Products.	**07**
	(b)	What are the considerations to be taken into account when designing mixed signal circuit board using PSoC 5LP ?	**07**
		OR	
	(b)	Explain how PSoC creator, PSoC Components and PSoC Systems together help Hardware-Software codesign of Embedded SoC.	**07**
Q.3	**(a)**	Give a brief overview of Xilinx-Zynq-7000 All Programmable SoC.	**07**
	(b)	(i) Briefly describe simulation steps in a VHDL based design.	**03**
		(ii) Give brief description about Qualcomm Snapdragon SoC.	**04**
		OR	
Q.3	**(a)**	Explain the NEON SIMD architecture. Also describe, using a suitable diagram, how the instruction VADD.I16 Q0, Q1, Q2 is executed on the NEON architecture.	**07**
	(b)	(i) What are the options for interfacing external processor to an Altera FPGA ?	**03**
		(ii) What are the steps taken to achieve power efficiency in an SoC design.	**04**
Q.4	**(a)**	What are the key points in designing Dynamic Memory Controller using FPGA core ?	**07**
	(b)	What do you understand by TLM ? Briefly explain its methodology.	**07**
		OR	
Q.4	**(a)**	What is a cross compiler ? Explain its uses in the context of Embedded system design using FPGA cores and SoC.	**07**
	(b)	Draw the block diagram showing basic constituents of SoC design flow and briefly elaborate the requirement analysis process.	**07**

Q.5	**(a)**	(i) What are the advantages of implementing custom instructions in FPGA based processor ?	**03**
		(ii) Explain the seven different sources of exceptions in Zinq SoC.	**04**
	(b)	(i) What do you understand by "channel" in SystemC. List down various channels available in SystemC and explain any two channels briefly.	**03**
		(ii) Explain the power supply pins of PSoC 4	**04**

OR

Q.5	**(a)**	(i) Briefly describe the booting process in a stand alone embedded system with a processor.	**03**
		(ii) Explain the process of implementing a floating-point matrix multiplication accelerator using Zynq SoC platform.	**04**
	(b)	(i) What are the special challenges in SoC verification ?	**03**
		(ii) Draw the block diagram of Analog and Digital Layout in PSoC 5LP and explain with reason which ports are the best analog ports.	**04**

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