Seat No.: _____ Enrolment No._____

GUJARAT TECHNOLOGICAL UNIVERSITY

ME – SEMESTER III (NEW) • EXAMINATION – SUMMER 2016

Subject Code: 3735201 **Date: 05/05/2016**

Subject Name: Design for Testability

Time:10:30 am To 01:00 pm **Total Marks: 70**

Instructions:

1. **Attempt all questions.**
2. **Make suitable assumptions wherever necessary.**
3. **Figures to the right indicate full marks.**

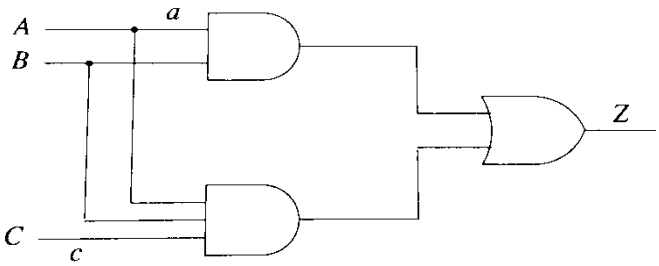
Q.1 **(a)** What is the difference between verification and DFT? **07**

(b) For the circuit shown in Figure **07**

(i)Find the set of all tests that detect the fault c s - a – 1.

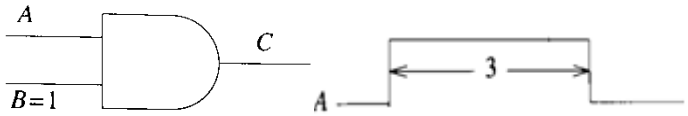
(ii)Find the set of all tests that detect the fault a s - a – 0

(iii)Find the set of all tests that detect the multiple faults {c s-a-1, a s-a-0}



Q.2 **(a)** What is the difference between structural and functional vectors? **07**

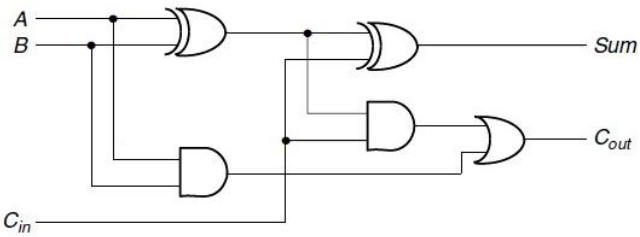
(b) Analyze the propagation of the pulse at A shown in figure for the following rise and fall delays of gate C: (i) d_r=3,d_f=1;(ii) d_r=4,d_f=1; (iii)d_r=5,d_f=1 **07**



OR

(b) Construct a truth table for an XOR function of two input using the five logic values 0, 1, x, D, and D'. **07**

Q.3 **(a)** Calculate Controllability & Observability for below circuit? **07**



(b) What the major problem faced in DFT with Bi-Directional I/O Ports and how is it resolved. **07**

OR

Q.3 **(a)** What is Pseudo-Random testing? Describe? **07**

(b) Discuss the various methods to block unknown(X) source? **07**

Q.4	(a)	What are typical faults in the memory cell array? Discuss all of them?	07
	(b)	Write the short note on following: (i) Syndrome Drive counter, (ii) Constant – weight counter, and (iii) Combined LFSR/SR.	07
		OR	
Q.4	(a)	Brief note on (i) LOCSTand (ii)CSBL.	07
	(b)	What are RAM dynamic faults? Discuss?	07
Q.5	(a)	Discuss 2D RAM redundancy allocation operation with diagram?	07
	(b)	What is BISR? What are advantages BIRA over BISR?	07
		OR	
Q.5	(a)	What is TAP controller? Describe its state Diagram, function and States?	07
	(b)	Briefly discuss about following BSCAN test Architectures (i)Ring architecture (ii)Multi-drop architecture,(iii)Hierarchical architecture.	07

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