Seat No.: _____ Enrolment No._____

GUJARAT TECHNOLOGICAL UNIVERSITY

ME – SEMESTER I (OLD) – • EXAMINATION – SUMMER 2016

Subject Code: 710403N **Date:18/05/2016**

Subject Name: ASIC Design

Time:02:30 pm to 05:00 pm **Total Marks: 70**

Instructions:

1. **Attempt all questions.**
2. **Make suitable assumptions wherever necessary.**
3. **Figures to the right indicate full marks.**

Q.1 **(a)** Give answer of following questions. **07**

(i) List the major capabilities of VHDL along with the features that differentiate it from other hardware description languages.

(ii) Explain VHDL terms: Configuration, Package, Generic and Process.

(b) Discuss VLSI design methodology. Distinguish between top - down and bottom - up design methodologies for digital design. **07**

Q.2 **(a)** Give answer of following questions. **07**

(i) Compare Inertial and Transport delay with suitable examples and explain Inertial Delay Model.

(ii) What is Delta-delay? What is its effect in VHDL?

(b) Explain the ASIC Design flow in brief. Also explain Full custom and Semi custom mask layout. **07**

OR

(b) Write True or False. If statement is true justify it and if false correct it. **07**

(i) The order of execution of concurrent VHDL statements cannot be predicted.

(ii) The statement a<=b after 5 ns; is synthesized as a delay line of 5 ns.

(iii) One entity may be assigned to many architecture bodies.

(iv) We cannot mix structural and data flow description in the same architecture unit.

(v) Structural style is closer to human thinking than behavioral style.

(vi) Every signal in a sensitivity list of a statement must change to fire the statement.

(vii) RTL style describes combinational logic.

Q.3 **(a)** Write a VHDL code for 16 input priority encoder with Truth Table. **07**

(b) Write a VHDL code for 4 bit shift right register using generate statement. **07**

OR

Q.3 **(a)** Write a VHDL code for 4x1 multiplexer using when else construct. Using same draw diagram and write VHDL code to implement 16x1 multiplexer using structural modeling. **07**

(b) Write VHDL code for 2x4 decoder using process. Using 2x4 decoder draw and write VHDL code to implement 3x8 decoder using structural modeling. **07**

Q.4 **(a)** Explain Test Bench with example. **07**

(b) Briefly describe implicit and explicit visibility in VHDL. **07**

OR

Q.4 **(a)** Explain modeling of finite state machines. Also compare Moore state Machines and Mealy state machines. **07**

	(b)	Explain following operators used in VHDL with example (1) rem (2) mod (3) abs	**07**
Q.5	**(a)**	Draw and Explain CPLD Architecture.	**07**
	(b)	Explain PLA with necessary Diagrams and equations.	**07**

OR

Q.5	**(a)**	Write a short note on Technology mapping for FPGA .	**07**
	(b)	Explain Design Implementation using FPGA with appropriate example.	**07**

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