Seat No.: _____ Enrolment No._____

GUJARAT TECHNOLOGICAL UNIVERSITY

ME - SEMESTER– II(Old course) • EXAMINATION (Remedial) – WINTER- 2015

Subject Code: 1710412 **Date: 16/12/2015**

Subject Name: Digital VLSI Design

Time:2:30 pm to 5:00 pm **Total Marks: 70**

Instructions:

1. **Attempt all questions.**
2. **Make suitable assumptions wherever necessary.**
3. **Figures to the right indicate full marks.**

Q.1	**(a)**	Fill in the Blanks. (One mark each)	**07**
	1	Let resistance and capacitance of transistor are R and C respectively. If width of transistor increase by factor k new value of resistance = _____ and capacitance = _____ in terms of R and C.	
	2	In CMOS if NMOS and PMOS transistors are of same size, fall time is _____ than rise time.	
	3	Let Vg is gate voltage = V_{DD} and Vs is source voltage = V_{DD} then, maximum output voltage of NMOS pass transistor is _____	
	4	Distance between drain to source is _____ in 300nm process.	
	5	In terms of power dissipation static circuits dissipate _____ power than dynamic circuits.	
	6	If noise margin of gate increases, noise immunity of gate will _____	
	(b)	Answer the following in short. (One mark each)	**07**
	1	Explain Feature size.	
	2	Which methods are used for n-well formation?	
	3	Where substrate of CMOS must be tied?	
	4	Which pass transistor produces strong 1?	
	5	Compare static and dynamic circuits for speed of operation.	
	6	How we can model gate capacitor of MOS transistor?	
	7	What do you mean by Pseudo gate?	
Q.2	**(a)**	Draw Circuit diagram and stick diagram for boolean function Y1 = $\overline{AB + C}$ Y2 = $\overline{ABC}$	**07**
	(b)	Explain fabrication steps of CMOS inverter with necessary diagram	**07**
		OR	
	(b)	Explain types of photoresists and their usage in lithography process with appropriate diagram.	**07**
Q.3	**(a)**	Explain RC delay model for CMOS inverter with appropriate diagram and explain how rise time and fall time are computed if inverter is driving another inverter.	**07**
	(b)	Explain the nMOS and pMOS enhancement transistor with its physical structure	**07**
		OR	
Q.3	**(a)**	Sketch transistor level schematic for following Boolean function, and identify size of transistor so that rise and fall time of logic gate is approximately same. Y1 = $\overline{ABC + D}$ Y2 = $\overline{(AB + C)\,D}$	**07**
	(b)	Draw energy band diagram of the combined MOS system. Explain MOS system under different external bias voltage with energy band diagram.	**07**
Q.4	**(a)**	Explain operation of MOS transistor in various regions and derieve equations for drain to source current.	**07**

	(b)	Calculate the delay time for CMOS inverter during its high to low transition.	**07**
		OR	
Q.4	**(a)**	Discuss noise margin of CMOS inverter with transfer characteristic.	**07**
	(b)	Explain with circuit two input CMOS NOR and NAND gate. Also derive threshold voltage for both.	**07**
Q.5	**(a)**	Write a short note on CMOS Transmission Gate. Explain its usefulness.	**07**
	(b)	Explain 2 input NAND Gate using CMOS, pass and CPL logic.	**07**
		OR	
Q.5	**(a)**	Draw MOS transistor level schematic and explain operation of D Latch as well D Flip-flop with waveforms.	**07**
	(b)	Compare static and dynamic NOR gate with appropriate diagram.	**07**

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