Seat No.: _____ Enrolment No._____

GUJARAT TECHNOLOGICAL UNIVERSITY

ME - SEMESTER– II(Old course) • EXAMINATION (Remedial) – WINTER- 2015

Subject Code: 1720302 **Date: 10/12/2015**

Subject Name: Advance Instrumentation

Time:2:30 pm to 5:00 pm **Total Marks: 70**

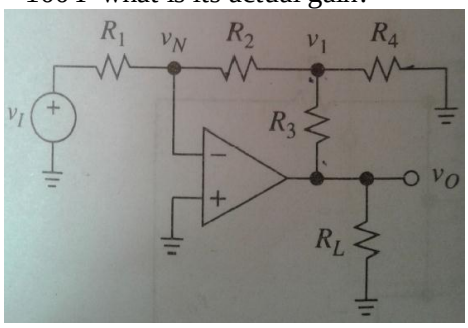
Instructions:

1. **Attempt all questions.**
2. **Make suitable assumptions wherever necessary.**
3. **Figures to the right indicate full marks.**
4. **All symbols carry their usual meaning unless otherwise stated.**
5. **Draw all necessary circuit diagrams in your solution.**
6. **Show all necessary node voltages and currents, while deriving equations.**

Q.1 For the circuit shown in following figure let $R_1 = R_2 = 1$ MÝ, $R_3 = 100$ kÝ, $R_4 = 1$ kÝ, and $R_L = 1$ kÝ. **14**

(a) Derive the equation of ideal gain A and evaluate the same.

(b) Derive the equation of actual gain of circuit. If the op amp has $r_d = 1$ MÝ, $a = 10^5$ V/V, and $r_0 = 100$Ý what is its actual gain?



Q.2 **(a)** Draw the circuit diagram of dual-op-amp instrumentation amplifier (IA) with variable gain and derive the equation of its gain considering virtual ground condition. What is the limitation of this IA compared to triple-op-amp configuration? **07**

(b) Draw the circuit diagram of high-sensitivity I-V converter and derive the equation of gain. Design the circuit for the sensitivity of 0.1 V/nA. **07**

OR

(b) What do you mean by voltage compliance of the circuit? In a floating load V-I converter (non-inverting mode) $v_I = 5$V, R = 10 kÝ, $\pm$ Vsat = $\pm$ 15 V, and resistive load R_L. Find the current i_O passing through the load, the voltage compliance, and the maximum permissible value of R_L. **07**

Q.3 **(a)** An inverting amplifier with $R_1 =$ 10 kÝ, $R_2 = 20$ kÝ, and $v_I = 3$ V drives a 2 kÝ load. (a) Assuming $I_Q = 0.5$ mA, find i_{CC}, i_{EE}, and i_O. (b) Find the power dissipated inside the op-amp. **07**

(b) Draw the circuit diagram of bridge linearization by constant - current drive and derive the equation of output voltage. **07**

OR

Q.3 Draw the circuit diagram of strain-gauge bridge, having four strain-gauges, **14**

connected with instrumentation amplifier (IA), referred to as a load cell, and having calibration facility to account for gauge resistances and reference voltage.

i. Derive the relationship of output voltage with gain of IA, reference voltage, and fractional change in resistance ŭ.

ii. Let the strain-gauges be of 120 Ý ± 1 % types and their maximum power dissipation limited to 25 mW to avoid excessive self heating. Assume that VREF = 10V ± 5%, specify suitable values for R_1 through R_4 used for calibration.

iii. Outline the calibration procedure.

Q.4 Draw the circuit diagram of second order high-pass KRC filter and derive the equations of gain, cutoff frequency and Q-factor. Write the equations for equal component design. **14**

OR

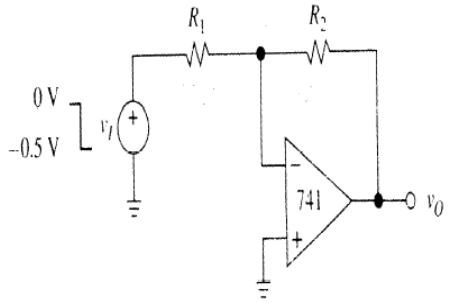
Q.4 How can we use switched capacitor (SC) as resistor? Describe SC integrators and practical limitations of SC filters with the help of circuit diagrams and waveforms. **14**

Q.5 (a) What do you mean by unconditionally stable op amp? With the help of necessary diagram and equations explain the role of feedback pole to raise phase margin of the op amp circuit. **07**

(b) Explain input bias and input offset currents. Derive the equation of error voltage generated due to the input bias current and input offset current for the resistive feedback op amp circuit. What are the ways to reduce this error voltage? What are the consequences of these ways? **07**

OR

Q.5 Illustrate slew rate with the help of necessary waveforms and derivations. An op amp shown in following figure has an input bias current of 20 µA and a compensation capacitance Cc of 30 pF, and slew rate of 0.5 V/µs, find its response $v_O(t)$ to a step input of -0.5 V. Consider R_1 = 3 kÝ and R_2 = 12 kÝ. **14**



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