Seat No.: _____ Enrolment No._____

GUJARAT TECHNOLOGICAL UNIVERSITY

ME - SEMESTER–I(New course)• EXAMINATION – WINTER- 2015

Subject Code: 2710507 **Date: 01/01/2016**

Subject Name: ASIC Design

Time:2:30 pm to 5:00 pm **Total Marks: 70**

Instructions:

1. **Attempt all questions.**
2. **Make suitable assumptions wherever necessary.**
3. **Figures to the right indicate full marks.**

Q.1 **(a)** Answer the following **06**

i) List major capabilities of VHDL

ii) Describe different levels of abstraction in HDL

(b) Do as directed **08**

i) Declare entity for 4×1 MUX

ii) List nine values of std_logic

iii) Differentiate between concurrent and sequential statements

iv) Can you have process statement without sensitivity list? Explain

Q.2 **(a)** Draw a flow chart indicating major steps involved in chip design using CAD tools. **07**

(b) Write behavioral VHDL code for BCD to 7 Segment decoder **07**

OR

(b) Write a behavioral VHDL code for 8 bit shift register with parallel loading and shift left-right control **07**

Q.3 **(a)** i) Compare inertial and transport delay models with necessary examples **07**

ii) What is delta delay? What is its effect in VHDL?

(b) i) Describe various WAIT statements. **07**

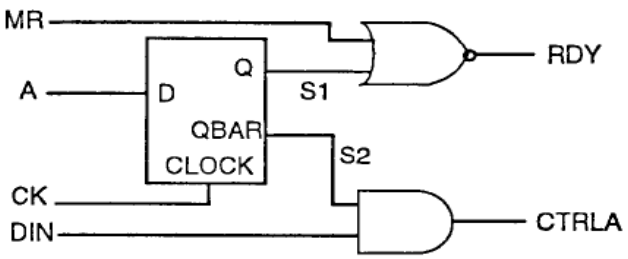
ii) Using WAIT statement, write VHDL code for asynchronous reset D flip flop

OR

Q.3 **(a)** List main purposes of test bench. Discuss waveform generation using test bench **07**

(b) Discuss types of Finite State Machine (FSM) with appropriate example **07**

Q.4 **(a)** Write VHDL code for circuit given below **07**



(b) Write VHDL code for 9 bit parity generator **07**

OR

Q.4 **(a)** Explain component declaration and component instantiation statement **07**

(b) Write VHDL code using structural model for a 4 bit full adder **07**

Q.5	**(a)**	Draw architecture or block diagram of one of the FPGA and explain its working	**07**
	(b)	Write short note on floor planning and placement	**07**
		OR	
Q.5	**(a)**	Draw architecture or block diagram of one of the CPLD and explain its working	**07**
	(b)	Discuss fuse and anti fuse technology of FPGA programming with appropriate diagram	**07**

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